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AN ADVANCED LOAD SHARING AND CIRCULATING CURRENT MINIMIZATION BY VOLTAGE QUADRUPLER FOR HIGH OUTPUT-VOLTAGE GAIN CONVERTERS FED STANDALONE MICRO GRID

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ABSTRACT:

An advanced symmetrical voltage quadrupler rectifier (SVQR) is derived in this paper to serve as the secondary rectification topology, which helps to extend the converter voltage gain and reduce the output diode voltage stresses. The output voltage is four times of the conventional full-bridge voltage rectifier with the same transformer ratio, which benefits to reduce the turns ratio of the transformer and decrease the parasitic parameters. Also, low voltage-rated diodes with high switching performance can be applied to improve the efficiency. Meanwhile, all the diodes in SVQR have the same voltage and current stresses, which simplifies the thermal design. Furthermore, two output electrolytic capacitors are connected in series to share the high output voltage, and the voltage balance can be realized naturally without any additional voltage-sharing scheme.

INTRODUCTION:

NOWADAYS, photovoltaic (PV) power generation systems are getting more and more widespread with the increasing energy demand and the concern for the worldwide environmental pollution. However, in the PV generation systems, the output voltages of the sources, such as the PV panels and batteries, are usually lower than 50 V, while 380-V dc-bus voltage is needed to supply the grid for a single-phase full-bridge inverter. Especially, 760-V dc-bus voltage is required in the half-bridge inverter, neutral point clamp inverter, and three-phase four-wire inverter. Therefore, in the centralized system, the PV panels are usually series connected in order to generate

sufficiently high voltage. However, when the partial shading happens, the maximum power point track losses are increased considerably, and the lifetime of the panel is reduced due to the hot-spot effect. Modular systems are introduced to solve the aforementioned problems, where an independent converter is applied to each PV panel to maximize the output power and avoid panel hot-spot risk.

TOPOLOGY DERIVATION AND OPERATIONAL PROCESSES:

In this paper, an advanced symmetrical voltage quadrupler rectifier (SVQR) is derived from the half-wave voltage doubler for the high output voltage and high step-up dc–dc conversion applications. The output voltage is four times of the conventional full-bridge voltage rectifier, which helps to reduce the turns of the secondary winding and decrease the parasitic parameters of the transformer. Meanwhile, the device voltage stress is half of the output voltage. Therefore, low voltage-rated and high performance diodes can be applied to improve the converter efficiency. Moreover, the output capacitor voltage balance can be realized naturally, which makes the voltage quadrupler more suitable for the 760 V dc-bus-based grid-connected PV generation systems due to the relatively low voltage of the aluminum electrolytic capacitors. In addition, all the diode current stresses are the same, which simplifies the system thermal design. The derived SVQR can be taken as a fundamental rectification configuration for future large voltage conversion and high output voltage applications.

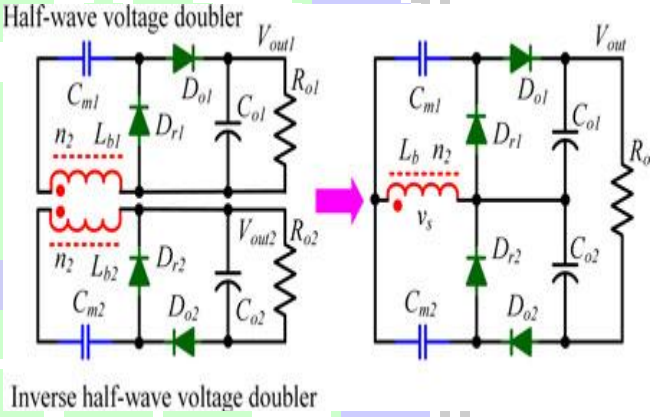


Fig. 1. Derivation of the SVQR.

As shown in Fig. 1, SVQR can be derived by combining a half-wave voltage doubler rectifier and its inverse type with the shared secondary winding. In the introduced SVQR, Cm1 and Cm2 are the series capacitors; Co 1 and Co 2 are the output capacitors; Dr 1 and Dr 2 are the regenerative diodes; Do 1 and Do 2 are the output diodes; Lb is the secondary winding

and vs is the voltage across Lb ; Vout is the output voltage; and Ro is the load. The circuit performance comparison between the voltage doublers and SVQR is shown in Table I. Assuming that the value of secondary winding voltage vs can be +Vs , −Vs , and zero in one switching cycle, the output voltage of SVQR Vout is four times of Vs , which benefits to reduce the number of turns greatly on the secondary side compared with the voltage doubler circuits. The voltage stresses on the diodes and the capacitors are half of the high output voltage. Therefore, low voltage-rated and good performance diodes can be adopted to improve the converter efficiency.

TABLE I

PERFORMANCE COMPARISON BETWEEN VOLTAGE DOUBLER AND SVQR

Rectifier circuit	Half-wave voltage doubler	Full-wave voltage doubler	SVQR
Output voltages (V_{out})	$2V_s$	$2V_s$	$4V_s$
Diode voltage Stress (V_D)	V_{out}	V_{out}	$V_{out}/2$
Diode current stress (I_D)	I_o	I_o	I_o
Capacitor voltage stress (V_{Co})	V_{out}	V_{out}	$V_{out}/2$

B. Operational Process Analysis

In order to easily explain the operational process and the circuit performance of SVQR, the conventional dual boost converter is employed in the primary side as a typical example. The dual boost converter with SVQR is plotted in Fig. 2, where and are the main switches; and are the filter inductors; and is the primary winding of the transformer. The transformer can be equivalent to a leakage inductor in series with an ideal transformer. N is defined as the turns ratio / . As shown in the dashed block, the active clamp circuits are introduced to recycle the leakage inductance energy and make all the switches work with zero-voltage-switching (ZVS) turn-on condition. $_1$ and $_2$ are the clamp switches; and $_1$ and $_2$ are the clamp capacitors. $_1$ and $_2$ are the parallel capacitors to reduce the turn-off losses for the switches.

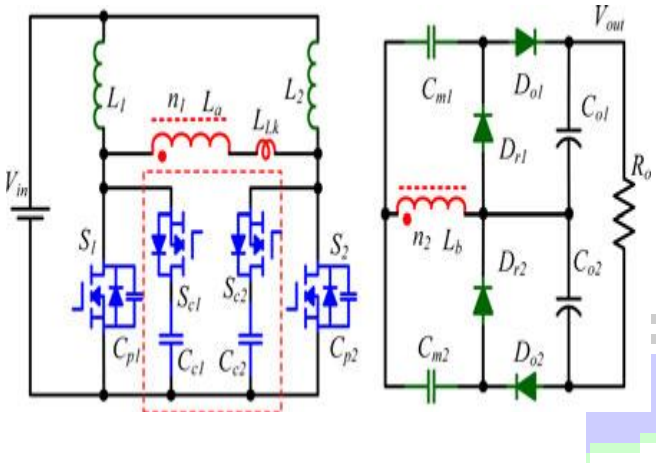


Fig. 2. Isolated dual boost converter with SVQR and active clamp scheme.

Stage 1 [t0 –t1]: Before t1 , main switches S1 and S2 are in the ON state, and clamp switches Sc 1 and Sc 2 are in the OFF state. All the secondary-side diodes Dr 1 , Dr 2 , Do 1 , and Do 2 are reverse-biased. The current of the filter inductors L1 and L2 is caused by the input voltage to increase linearly.

Stage 2 [t1 –t2]: At t1 , main switch S1 turns OFF, and then the parallel capacitor Cp 1 is charged by the filter inductor current iL 1 . The voltage on Cp 1 increases almost with a constant slope. The voltage increasing rate across switch S1 is limited by the parallel capacitor Cp 1 , which reduces the turn-off losses effectively.

Stage 3 [t2 –t3]: At t2 , the voltage across main switch S1 is high enough to cause the anti-parallel diode of clamp switch Sc 1 to conduct. Then, the voltage of main switch S1 is clamped to the voltage on Cc 1 . Because Cc 1 is much larger than Cp 1 , most of the filter inductor current flows through Cc 1 .

Stage 4 [t3 –t4]: At t3 , the voltages across secondary-side diodes Do 1 and Dr 2 fall to zero, and then, the energy is transferred to the series capacitor Cm2 and output capacitor Co 1 through the transformer. Series capacitors Cm1 , Cm2, clamp capacitor Cc 1 , and leakage inductance of the transformer LLk form a resonant circuit. Since the resonant period is relatively large, the current of LLk increases almost linearly.

Stage 5 [t4 –t5]: The turn-on signal of Sc 1 is given at t4 . The clamp switch turns ON when its antiparallel diode is in the ON state. Thus, the ZVS-on condition of the clamp switch is realized. The equivalent circuit in this stage is similar to that of previous one.

Stage 6 [t5 –t6]: The clamp switch Sc 1 turns OFF at t5 . Then, the clamp capacitor

Cc 1 is disconnected from the resonant circuits. LLk and Cp 1 form a new resonant circuit. The decreasing rate of the leakage current is almost constant due to the relatively large resonant period. The energy stored in Cp 1 is transferred to LLk. The voltage increasing rate of Sc 1 is limited by Cp 1 , which helps in reducing the turn-off losses.

Stage 7 [t6 –t7]: The voltage on Cp 1 falls to zero at t6 , and the antiparallel diode of S1 begins to conduct. Cp 1 and LLk stop resonating. The current through LLk decreases linearly, which controls the current falling rate of secondary-side diodes Do 1 and Dr 2 .

Stage 8 [t7 –t8]: At t7 , the turn-on signal is applied to the main switch S1 when its antiparallel diode is in the ON state, and S1 turns ON with ZVS. The current through LLk falls to zero at t8 , and after that, the secondary-side diodes are reversed-biased, and L1 is charged by the input voltage again.

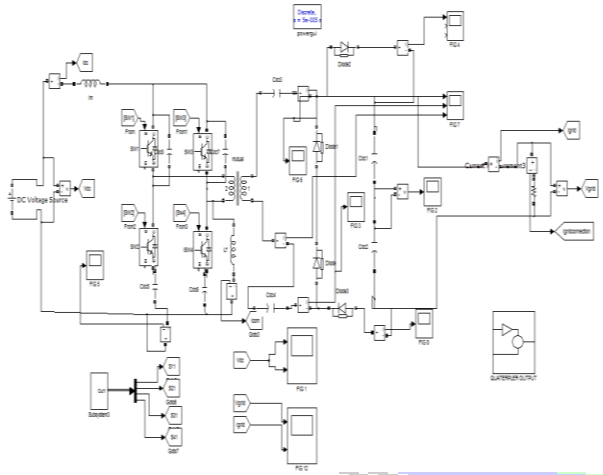
C. Topology Variation and Comparison

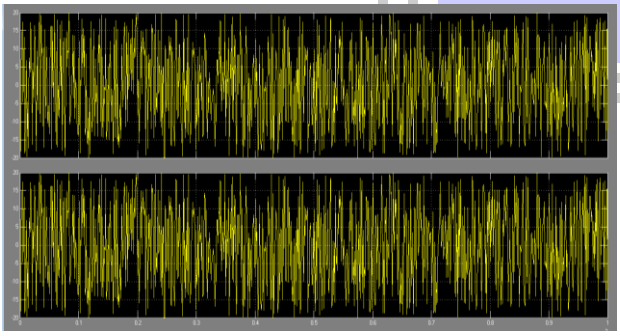
The half-wave voltage doubler circuit can be used as a basic voltage rectifier cell to derive other voltage multiplier structures. Besides the aforementioned SVQR shown inFig.3(a), there are other three kinds of voltage quadrupler with different connection methods. As shown in Fig. 3(b), the CW voltage quadrupler can be considered as two series-connected half-wave voltage doubler cells. By combining one full-wave voltage doubler and one half-wave voltage doubler cell, two asymmetrical voltage quadrupler circuits are derived in Fig. 3(c) and. In fig 3 the components are annotated uniformly for better understanding. The performance comparison among these voltage quadrupler circuits is shown in Table II. It can be seen that the numbers of the component and the component voltage stresses in these four voltage quadrupler rectifiers are the same. Voltage quadrupler rectifier A (VQR A) has the largest total diode current stress. Fortunately, the total diode current stress of SVQR is the lowest among these quadrupler rectifiers. The current ripples of the capacitors in different types of voltage quadruplers are similar to that of the diodes. The SVQR has the smallest total capacitor current stress among these four circuits, while VQR A has the largest one. Therefore, with the same output voltage ripples, SVQR has the lowest losses and cost. Sometimes, the withstanding voltage of the transformer needs to be considered in the system design. When the output voltage is separated into a positive bus voltage and a negative one, the SVQR structure has the lowest transformer withstanding voltage.

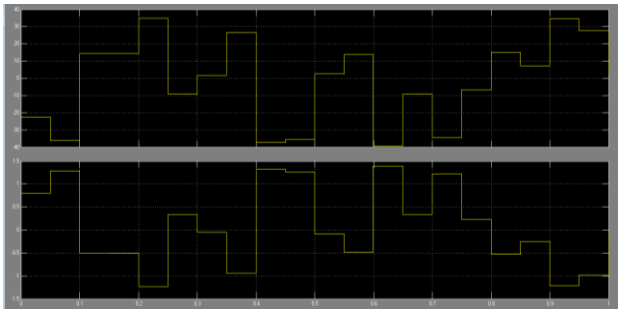
TABLE II
PERFORMANCE COMPARISON AMONG VOLTAGE QUADRUPLER CIRCUITS

Rectifier circuit	VQR A	VQR B	VQR C	SVQR
Number of diodes	4	4	4	4
Number of capacitors	4	4	4	4
Diode voltage stress (V_D)	$V_{out}/2$	$V_{out}/2$	$V_{out}/2$	$V_{out}/2$
Current stress of D_1 (I_{D1})	$2I_o$	I_o	I_o	I_o
Current stress of D_2 (I_{D2})	$2I_o$	$2I_o$	I_o	I_o
Current stress of D_3 (I_{D3})	I_o	I_o	$2I_o$	I_o
Current stress of D_4 (I_{D4})	I_o	I_o	I_o	I_o
Total diode current stress (ΣI_D)	$6I_o$	$5I_o$	$5I_o$	$4I_o$

SIMULATION MODEL WITH RESULTS







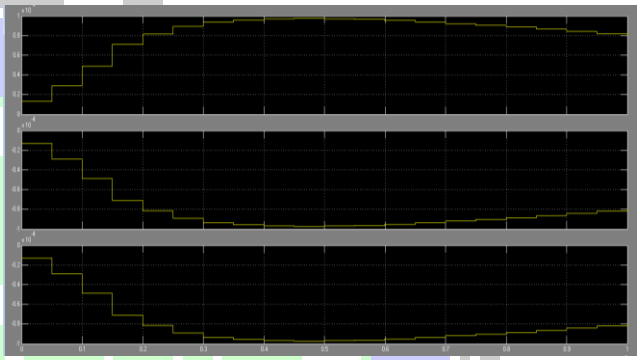


Fig .3 matlab model : (a)(b)(c) voltages of Vdc, grid & voltage gain

CONCLUSION

An advanced SVQR derived from half-wave voltage doubler circuit is introduced in this paper to satisfy high output voltage and voltage gain PV dc modular distributed applications. The voltage stress of the component in SVQR is reduced to half of the output voltages. Meanwhile, the voltage conversion ratio is improved greatly. The SVQR configuration can extend the voltage conversion ratio of the converter, which makes it more suitable for high step-up applications. The output

capacitor voltages are balanced naturally. Dual boost with active clamp scheme is adopted as the primary circuit for better understanding the operational processes of SVQR. The performance analyses and experimental results show SVQR competitive solution as the secondary-side rectification circuits in the high voltage conversion applications. One of the main contributions of this paper is to derive advanced universal voltage quadrupler rectifier configurations for next-generation high step-up and high-efficiency dc-bus-coupled PV distributed system.

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