Improvement Of Power Factor By Voltage Controlled Adjustable Speed PMBLDCM Drive

P Bhaskar*¹, : Tajuddin Sayyad² : Dr. Abdul Ahad³

¹M.tech (P.E) Student Department Of EEE, Nimra College Of Engineering & Technology

² Asst. Professor Department Of EEE, Nimra College Of Engineering & Technology

³Professor & Head Of The Department, Nimra College Of Engineering & Technology

Abstract: In this paper, a half-bridge DC-DC converter is used as a single-stage power factor correction (PFC) converter for feeding a voltage source inverter (VSI) based permanent magnet brushless DC motor (PMBLDCM) drive. The front end of this PFC converter is a diode bridge rectifier (DBR) fed from single-phase AC mains. The fly-back PFC converter is operated with the current multiplier control and voltage follower control schemes for improvement of power quality (PQ) at ac mains while controlling the operation of PMBLDCMD in wide range of speeds and input AC voltage variation.

INTRODUCTION:

Today more and more variable speed drives are designed into appliance products to increase product performance and system efficiency. The low dynamic drive, whereby the load or speed is changed quite slowly in comparison with the system mechanical time constant, is a solution for many common appliance applications because simple algorithms can perform the control tasks. Moreover, the necessary computing power can be minimized by using dedicated on chip peripheral modules (such as A/D converter, dedicated PWM outputs, input capture and output compare functions).

Three phase Brushless DC (BLDC) motors are good candidates because of their high efficiency capability and easy to drive features. The disadvantage of this kind of motor is the fact that commutation of motor phases relies on its rotor position. Although the rotor position is usually sensed by sensors, there are applications that require sensorless control. Benefits of the sensorless solution are elimination of the position sensor and its connections between the control unit and the motor.

PROPOSED POWER FACTOR IMPROVEMENT SCHEME OF PMBLDC

For the proposed voltage controlled drive, a half-bridge DC-DC converter is selected because of its high power handling capacity as compared to the single switch converters.

Moreover, it has switching losses comparable to the single switch converters as only one switch is in operation at any instant of time. It can be operated as a single-stage power factor corrected (PFC) converter when connected between the VSI and the DBR fed from single-phase AC mains, besides controlling the voltage at DC link for the desired speed of the Air-Con compressor.

A detailed modeling, design and performance evaluation of the proposed drive are presented for an air conditioner compressor driven by a PMBLDC motor of 1.5 kW, 1500 rpm rating.

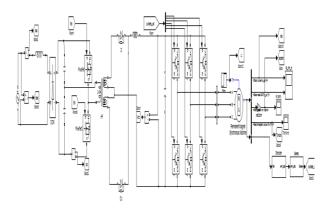


Figure 1. Flyback converter fed PMBLDCMD with current multiplier control

The proposed speed control scheme (as shown in Fig. 1) controls reference voltage at DC link as an equivalent reference speed, thereby replaces the conventional control of the motor speed and a stator current involving various sensors for voltage and current signals. Moreover, the rotor position signals are used to generate the switching sequence for the VSI as an electronic commutator of the PMBLDC motor. Therefore, rotor-position information is required only at the

commutation points, e.g., every 60°electrical in the three phase. The rotor position of PMBLDCM is sensed using Hall effect position sensors and used to generate switching sequence for the VSI as shown in Table-I. The DC link voltage is controlled by a half-bridge DC-DC converter based on the duty ratio (D) of the converter.

For a fast and effective control with reduced size of magnetic and filters, a high switching frequency is used; however, the switching frequency (fs) is limited by the switching device used, operating power level and switching losses of the device. Metal oxide field effect transistors (MOSFETs) are used as the switching device for high switching frequency in the proposed PFC converter. However, insulated gate bipolar transistors (IGBTs) are used in VSI bridge feeding PMBLDCM, to reduce the switching stress, as it operates at lower frequency compared to PFC switches. The PFC control scheme uses a current control loop inside the speed control loop with current multiplier approach which operates in continuous conduction mode (CCM) with average current control. The control loop begins with the comparison of sensed DC link voltage with a voltage equivalent to the reference speed. The resultant voltage error is passed through a proportional-integral (PI) controller to give the modulating current signal. This signal is multiplied with a unit template of input AC voltage and compared with DC current sensed after

the DBR. The resultant current error is amplified and compared with saw-tooth carrier wave of fixed frequency (fs) in unipolar scheme (as shown in Fig.2) to generate the PWM pulses for the half-bridge converter. For the current control of the PMBLDCM during step change of the reference voltage due to the change in the reference speed, a voltage gradient less than 800 V/s is introduced for the change of DC link voltage, which ensures the stator current of the PMBLDCM

within the specified limits (i.e. double the rated current).

MODELING OF FLYBACK PFC CONVERTER FED PMBLDCMD

The proposed PFC buck half-bridge converter is designed for a PMBLDCM drive with main considerations on PQ constraints at AC mains and allowable ripple in DC link voltage. The DC link voltage of the PFC converter is given as,

where N_1 , N_{21} , N_{22} are number of turns in primary, secondary upper and lower windings of the high frequency (HF) isolation transformer, respectively.

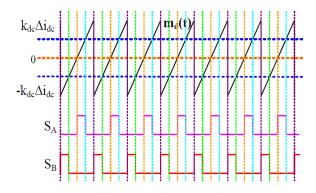


Figure 2. PWM control of the buck half-bridge converter

Vin is the average output of the DBR or a given AC input voltage (Vs) related as,

$$V_{in} = 2\sqrt{2V_S/\pi}$$
(2)

The main components of the proposed PMBLDCM drive are the PFC converter and PMBLDCM drive, which are modeled by mathematical equations and the complete drive is represented as a combination of these models.

A. PFC CONVERTER

The modeling of the PFC converter consists of the modeling of a speed controller, a reference current generator and a PWM controller as given below.

1) Speed Controller: The speed controller, the prime component of this control scheme, is a proportional-integral (PI) controller which closely tracks the reference speed as an equivalent reference voltage. If at kth instant of time, V*dc(k) is reference DC link voltage, Vdc(k) is sensed DC link voltage then the voltage error Ve(k) is calculated as,

$$V_e(k) = V_{dc}(k) - V_{dc}(k)$$
 (3)

The PI controller gives desired control signal after processing this voltage error. The output of the controller Ic(k) at k^{th} instant is given as,

$$\begin{split} I_{\text{c}}\left(k\right) &= I_{\text{c}}\left(k\text{-}1\right) + K_{\text{p}}\{V_{\text{e}}(k) - V_{\text{e}}(k\text{-}1)\} + K_{\text{i}}V_{\text{e}}(k)\\(4) \end{split} \label{eq:loss_equation}$$

Where Kp and Ki are the proportional and integral gains of the PI controller.

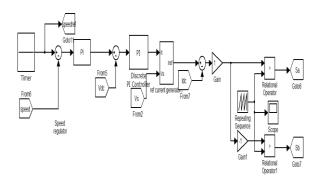


Figure.3 control scheme of proposed motor drive

2) **Reference Current Generator:** The reference input current of the PFC converter is denoted by idc* and given as,

$$i_{dc}^* = I_c (k) u_{V_5} \dots (5)$$

Where uVs is the unit template of the voltage at input AC mains, calculated as,

$$u_{Vs} = v_d/V_{sm}; v_d = |v_s|; v_s = V_{sm} \sin \omega t$$
. (6)

Where Vsm is the amplitude of the voltage and ω is frequency in rad/sec at AC mains.

3) PWM Controller: The reference input current of the buck half-bridge converter (idc*) is compared with its sensed current (idc) to generate the current error Δidc=(idc* - idc). This current error is amplified by gain kdc and compared with fixed frequency (fs) saw-tooth carrier waveform md(t) (as shown in Fig.2) in unipolar switching mode to get the switching signals for the MOSFETs of the PFC buck half-bridge converter as,

If
$$k_{dc} \Delta i_{dc} > m_d (t)$$
 then $S_A = 1$ else $S_A = 0$... (7)

If $-\mathbf{k}_{dc} \Delta i_{dc} > \mathbf{m}_{d} (t) \quad \text{then } \mathbf{S}_{B} = 1 \text{ else } \mathbf{S}_{B} = 0$(8)

Where SA, SB are upper and lower switches of the half-bridge converter as shown in Fig. 1 and their values '1' and '0' represent 'on' and 'off' position of the respective MOSFET of the PFC converter.

TABLE I. VSI SWITCHING SEQUENCE BASED ON THE HALL EFFECT

SENSOR SIGNALS

Ha Hb Hc Ea Eb Ec S1 S2 S3 S4 S5 S6

0	0	0	0 0 0	0	0
0	0	1 0	0 0 0	-1 1	+1 1
0	1 0	0 1	-1 1 0	+1 0	0
0	1 0	1 1	-1 0 0	0	+1
1	0 1	0 0	+1 0 1	0 0	-1 0
1	0 1	1 0	+1 0 0	-1 1	0 0
1	1 0	0	0 1 1	+1 0	-1 0
1 0	1 0	1 0	0 0	0 0	0 0

B. PMBLDCM DRIVE

The PMBLDCM drive consists of electronic commutators, a VSI and a PMBLDC motor.

- 1) Electronic Commutator: The electronic commutators uses signals from Hall effect position sensors to generate the switching sequence for the voltage source inverter based on the logic given in Table I.
- 2) Voltage Source Inverter: Fig. 3 shows an equivalent circuit of a VSI fed PMBLDCM. The output of VSI to be fed to phase 'a' of the PMBLDC motor is given as,

$$v_{ao} = (V_{dc}/2)$$
 for $S_1 = 1$ (9)

$$v_{ao} = (-V_{dc}/2)$$
 for $S_2 = 1$ (10)
 $v_{ao} = 0$ for $S_1 = 0$, and $S_2 = 0$ (11)
 $v_{an} = v_{ao} - v_{no}$ (12)

Where vao, vbo, vco, and vno are voltages of the three-phases and neutral point (n) with respect to virtual mid-point of the DC link voltage shown as 'o' in Fig. 2. The voltages van, vbn, vcn are voltages of three-phases with respect to neutral point (n) and Vdc is the DC link voltage. S= 1 and 0 represent 'on' and 'off' position of respective IGBTs of the VSI and considered in a similar way for other IGBTs of the VSI i.e. S3- S6.

Using similar logic vbo, vco, vbn, vcn are generated for other two phases of the VSI feeding PMBLDC motor.

3) **PMBLDC Motor**: The PMBLDCM is represented in the form of a set of differential equations given as,

$$v_{an} = Ri_a + p\lambda_a + e_{an}$$
 (13)
 $v_{bn} = Ri_b + p\lambda_b + e_{bn}$ (14)
 $v_{cn} = Ri_c + p\lambda_c + e_{cn}$ (15)

Where p is a differential operator (d/dt), ia, ib, ic are three-phase currents, λa , λb , λc are flux linkages and ean, ebn, ecn are phase to neutral back emf of PMBLDCM, in respective phases, R is resistance of motor windings/phase.

The flux linkages are represented as,

Where L is self-inductance/phase, M is mutual inductance of motor winding/phase. Since the PMBLDCM has no neutral connection, therefore,

$$i_a + i_b + i_c = 0$$
(19)

From Eqs. (14-21) the voltage between neutral terminal (n) and mid-point of the DC link (o) is given as,

$$v_{no} = \{v_{ao} + v_{bo} + v_{co} - (e_{an} + e_{bn} + e_{cn})\}/3$$
 (20)

From Eqs. (16-19), the flux linkages are given as,

$$\lambda_a = (L+M) i_a$$
, $\lambda_b = (L+M) i_b$, $\lambda_c = (L+M) i_c$,(21)

From Eqs. (13-15 and 21), the current derivatives in generalized state space form is given as,

$$pi_x = (v_{xn} - i_x R - e_{xn})/(L+M)$$
 (22)

Where x represents phase a, b or c.

The developed electromagnetic torque Te in the PMBLDCM is given as,

$$T_e = (e_{an} i_a + e_{bn} i_b + e_{cn} i_c) / \omega$$
 (23)

Where ω is motor speed in rad/sec,

The back emf may be expressed as a function of rotor position (θ) as,

$$e_{xn} = K_b f_x(\theta) \omega$$
 (24)

Where x can be phase a, b or c and accordingly $fx(\theta)$ represents function of rotor position with a maximum value ± 1 , identical to trapezoidal induced emf given as,

$$f_a(\theta) = 1$$
 for $0 < \theta < 2\pi/3$ (25)

$$f_a(\theta) = -1$$
 for $\pi < \theta < 5\pi/3$ (27)

$$f_a(\theta) = \{(6/\pi)(\theta - 2\pi)\} + 1 \text{ for } 5\pi/3 \le \theta \le 2\pi$$

.....(28)

The functions $fb(\theta)$ and $fc(\theta)$ are similar to $fa(\theta)$ with a phase difference of 120° and 240° respectively.

$$T_e = K_b \{ f_a(\theta) \ i_a + f_b(\theta) \ i_b + f_c(\theta) \ i_c \}$$
... (29)

The mechanical equation of motion in speed derivative form is given as,

$$p\omega = (P/2) (T_e - T_L - B\omega)/(J)$$
 (30)

The derivative of the rotor position angle is given as,

$$\mathbf{p}\mathbf{\theta} = \mathbf{\omega}$$
(31)

Where P is no. poles, TL is load torque in Nm, J is moment of inertia in kg-m2 and B is friction coefficient in Nms/Rad.

These equations (13-31) represent the dynamic model of the PMBLDC motor.

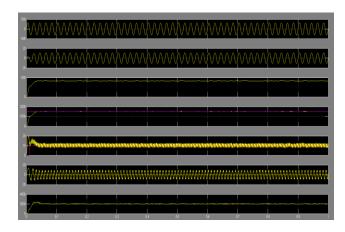
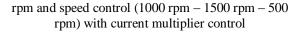


Figure.4 Simulated performance of flyback PFC converter fed PMBLDCMD during starting at 1000



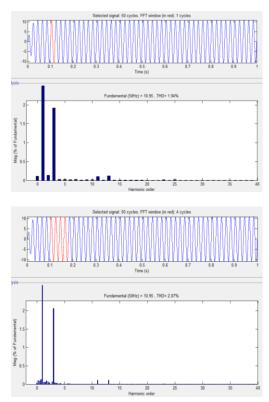


Figure.5 Current waveform at AC mains and its harmonic spectra of the PMBLDCM drive under steady state condition at rated torque and 220 VAC **CONCLUSION**

A new speed control strategy of a PMBLDCM drive is validated for a compressor load of an air conditioner which uses the reference speed as an equivalent reference voltage at DC link. The speed control is directly proportional to the voltage control at DC link. The rate limiter introduced in the reference voltage at DC link effectively limits the motor current within the desired value during the transient condition (starting and speed control). The design, modeling and simulation of flyback PFC converter fed PMBLDCM drive has been carried out in detail for its operation under speed control and varying input ac voltage. The CCM operation of the PFC converter under current multiplier control has shown better performance in terms of PO indices as compared to the voltage follower control operated in DCM operation of the PFC converter.

REFERENCES

- [1] T. Kenjo and S. Nagamori, Permanent Magnet Brushless DC Motors, Clarendon Press, oxford, 1985
- [2] T. J. Sokira and W. Jaffe, Brushless DC Motors: Electronic Commutation and Control, Tab Books USA, 1989.
- [3] J. R. Hendershort and T. J. E. Miller, Design of Brushless Permanent- Magnet Motors, Clarendon Press, Oxford, 1994.
- [4] J. F. Gieras and M. Wing, Permanent Magnet Motor Technology Design and Application, Marcel Dekker Inc., New York, 2002.
- [5] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," *IEEE Trans. Industrial Electron.*, vol. 50, no. 5, pp. 962 981, oct. 2003.
- [6] N. Mohan, T. M. Undeland and W. P. Robbins, "Power Electronics: Converters, Applications and Design," John Wiley and Sons Inc, USA, 1995.
- [7] J. Uceda, J. Sebastian and F.S. Dos Reis, "Power factor preregulators employing the flyback and zeta converters in FM mode," in *Proc. IEEE* Power Electronics Congress, 1996, pp. 132 137.
- [8] C. Larouci, J.P. Ferrieux, L. Gerbaud, J. Roudet and J. Barbaroux, "Control of a flyback converter in power factor correction mode: compromize between the current constraints and the transformer volume," in *Proc. IEEE APEC*, 2002, vol.2, pp. 722 727.

BIBLIOGRAPHY

Pothula Bhaskar Manikanta: pursuing M.Tech in Nimra College of engineering and technology, jupudi, Ibrahimpatnam. His specialization in power electronics. He graduated in Electrical and Electronics Engineering from Sri Venkateswara institute of science and information technology, Venkataramanagudem. Mail ID Bhaskarpothula@gmail.com

Tajuddin Sayyad: is currently working as an ASSISTANT PROFESSOR in Electrical and Electronics Engineering department at Nimra College of engineering and technology (NCET) jupudi, Ibrahimpatnam. He obtained his M TECH degree in Digital systems and computer electronics MAIL ID tajuddin.sayyad@gmail.com

DR.Abdul Ahad: Mtech. P.hd (NITK) is an eminent PROFESSOR & HEAD OF EEE, nimra group of colleges. he received M.Tech and was conferred Doctorate from NITK SURATKAL. He is expertised in power electronics, power systems, special Electrical machines& industrial machines, applications. He has over a 15 years of teaching experience .He trains various students for various competitive exams like IES ,IAS, GATE , AP GENCO, AP TRANSCO, DISCOMS and no of national competitive exams. He is the chair person of several national and technical symposiums. He published more than 20 international journals and attended several international conferences. His prime interest is in research .to his credit he guided scores of UG AND PG students in their projects and right now he is guiding two P,hd scholars.