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Analysis of Efficient CRC Implementation Configurations

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Abstract-A cyclic redundancy check (CRC) is an error-detecting code commonly used in digital networks and storage devices to detect accidental changes to raw data. Blocks of data entering these systems get a short check value attached, based on the remainder of a polynomial division of their contents; on retrieval the calculation is repeated, and corrective action can be taken against presumed data corruption if the check values do not match. Error correction codes provides a mean to detect and correct errors introduced by the transmission channel. A high-speed parallel cyclic redundancy check (CRC) implementation based on unfolding, pipelining, and retiming algorithms. CRC architectures are first pipelined to reduce the iteration bound by using novel look-ahead pipelining methods and then unfolded and retimed to design high-speed parallel circuits. The study and implementation using Verilog HDL. Modalism Xilinx Edition will be used for simulation and functional verification. Xilinx ISE will be used for synthesis and bit file generation. The Xilinx Chip scope will be used to test the results on Spartan 3E.

Keywords—*Cyclic redundancy checksum (CRC), digital logic, error detection,parallel,programmable.*

I-INTRODUCTION

Cyclic redundancy check is commonly used in data communication and other fields such as data storage, data compression, as a vital method for dealing with data errors. Usually, the hardware implementation of CRC computations is based on the linear feedback shift registers (LFSRs), which handle the data in a serial way. Though, the serial calculation of the CRC codes cannot achieve a high throughput. In contrast, parallel CRC calculation can significantly increase the throughput of CRC computations. For example, the throughput of the 32-bit parallel calculation of CRC-32 can achieve several gigabits per second however that is still not enough for high speed application such as Ethernet networks. A possible solution is to process more bits in parallel; Variants of CRCs are used in applications like CRC-16 BISYNC protocols, CRC32 in Ethernet frame for error detection, CRC8 in ATM, CRC-CCITT in X-25 protocol, disc storage, SDLC, and XMODEM.

II-CRC'S IN HIGH SPEED WIRELESS LAN

In networking environments, the cyclic redundancycheck (CRC) is widely utilized to determine whether errors have been introduced during transmissions over physical links. In this paper, we focus on the CRC calculation in WLAN where the packet size is huge and hence slow CRC calculation may become bottleneck for communication process. Based on this concept, paper present a novel implementation of the CRC implementation through multiple execution units that calculate CRC on different part of packet and then combine the result to get the final CRC. Consequently, the number of cycles utilized to recalculate the CRC codes is dramatically reduced. Furthermore, estimation on the maximum throughput is made based on synthesis results of our implementation and under that assumption, calculate actual CRC operation has been done. A performance study of the project is done by calculation of CRC with 2, 4, 8 execution units on same data block. There are several techniques for generating check bits that can be added to a message. Perhaps the simplest is to append a single bit, called the ―parity bit. Which makes the total number of 1-bits in the code vector.(message with parity bit appended) even (or odd). If a single bit gets altered in transmission, this will change the parity from even to odd (or the reverse). The sender generates the parity bit by simply summing the message bits modulo 2—that is, by exclusive or'ing them together. It then appends the

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parity bit (or its complement) to the message. The receiver can check the message by summing all the message bits modulo 2 and checking that the sum agrees with the parity bit. Equivalently, the receiver can sum all the bits (message and parity) and check that the result is 0 (if even parity is being used).This simple parity technique is often said to detect 1-bit errors. Actually it detects errors in any odd number of bits (including the parity bit), but it is a small comfort to know you are detecting 3-bit errors if you are missing 2-bit errors.

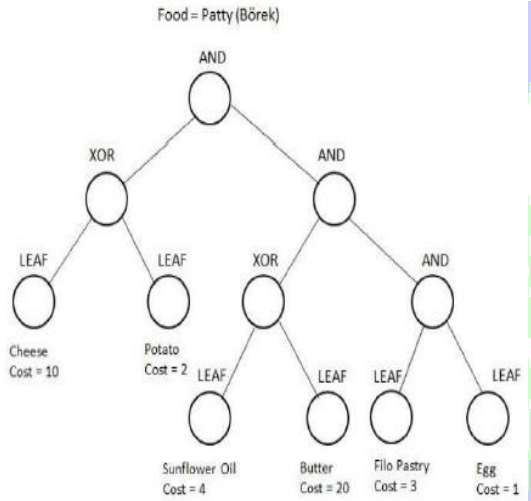

Fig.1. XOR Tree

Other techniques for computing a checksum are to form the exclusive or of all the bytes in the message, or to compute a sum with end-around carry of all the bytes. In the latter method the carry from each 8-bit sum is added into the least significant bit of the accumulator. It is believed that this is more likely to detect errors than the simple exclusive or, or the sum of the bytes with carry discarded. A technique that is believed to be quite good in terms of error detection, and which is easy to implement in hardware, is the cyclic redundancy check. This is another way to compute a checksum, usually eight, 16, or 32 bits in length that is appended to the message. We will briefly review the theory and then give some algorithms for computing in software a commonly used 32-bit CRC checksum. The CRC is based on polynomial arithmetic, in particular, on computing the remainder of dividing one polynomial in GF (2) (Galois field with two elements) by another. It is a little like treating the message as a very large binary number, and computing the remainder on dividing it by a fairly large prime such as intuitively, one would expect this to give a reliable checksum. A polynomial in GF (2) is a polynomial in a single variable x whose coefficients are 0 or 1. Addition and subtraction are done modulo 2—that is, they are both the same as the exclusive and operator. For example, the sum of the polynomials x3 + x + 1 and x4 +x3+ x2+ x is as is their difference. These polynomials are not usually written with minus signs, but they could be, because a coefficient of –1 is equivalent to a coefficient of 1. Multiplication of such polynomials is straightforward. The product of one coefficient by another is the same as their combination by the logical and operator, and the partial products are summed using exclusive or. Multiplication isnot needed to compute the CRC checksum. Division of polynomials over GF(2) can be done in much the same way as long division of polynomials over the integers. Below is an example.

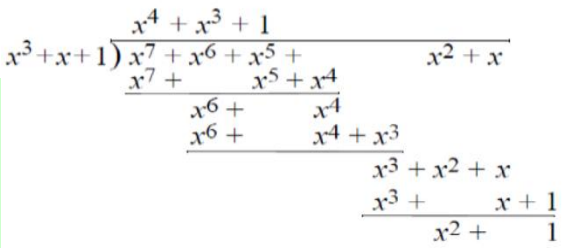

Fig.2. Division operation

The reader might like to verify that the quotient of multiplied by the divisor of x3+ x + 1 plus the remainder of equals the dividend. The CRC method treats the message as a polynomial in GF (2). For example, the message 11001001, where the order of transmission is from left to right (110…) is treated as a representation of the polynomialx7+ x6 + x3+ 1. The sender and receiver agree on a certain fixed polynomial called the generator polynomial. For example, for a 16-bitCRCtheCCITT(ComitéConsultatifInternationaleTélégraphique ET Téléphonique) 1 has chosen the polynomial x16 + x12+ x5 + 1 which is now widely used for a 16-bit CRC checksum. To compute an r-bit CRC checksum, the generator polynomial must be of degree r. The sender appends r 0-bits to the m-bit message and divides the resulting polynomial of degree m + r – 1 by the generator polynomial. This produces a remainder polynomial of degree r – 1 (or less). The remainder polynomial has r coefficients, which are the checksum. The quotient polynomial is discarded. The

data transmitted (the code vector) is the original m-bit message followed by the rbit checksum.

III-HARDWARE FEEDBACK SHIFT REGISTER

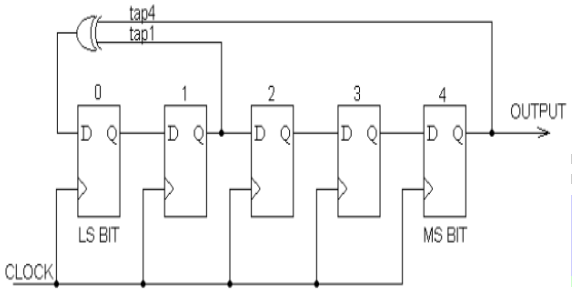

Fig.3. Feedback Shift Register

Initialize the CRC register to all 0-bits. Get first/next message bit m. If the high-order bit of CRC is 1, Shift CRC and m together left 1 position, and XOR the result with the low-order r bits of G. Otherwise, Just shift CRC and m left 1 position. If there are more message bits, go back to get the next one. CRC is playing a main role in the networking environment to detect the errors. With challenging the speed of transmitting data, to synchronize with speed, it's necessary to increase speed of CRC generation. Most electrical and computer engineers are familiar with the cyclic redundancy check (CRC). Many know that it's used in communication protocols to detect biterrors, and that it's essentially a remainder of the modulo-2long division operation. Some have had closer encounters with the CRC and know that it's implemented as a linear feedback shift register (LFSR) using flip-flops and XOR gates. They likely used an online tool or an existing example to generate parallel CRC code for a design.

In computing, a pipeline is a set of data processing elements connected in series, so that the output of one element is the input of the next one. The elements of a pipeline are often executed in parallel or in time-sliced fashion; in that case, some amount of buffer storage is often inserted between elements.

Retiming is the technique of moving the structural location of latches or registers in a digital circuit to improve its performance, area, and/or power characteristics in such a way that preserves its functional behavior at its outputs.

Unfolding is a transformation technique of duplicating the functional blocks to increase the throughput of the DSP program in such a way that preserves its functional behavior at its Outputs. Unfolding in general program is as known as Loop unrolling. Unfolding has applications in designing high-speed and low-power ASIC architectures. One application is to unfold the program to reveal hidden concurrency so that the program can be scheduled to a smaller iteration period, thus increasing the throughput of the implementation. Another Application is parallel processing in word level or bit level. Therefore these transformed circuit could increase the throughput and decrease the power consumption.

(a) Fast CRC:

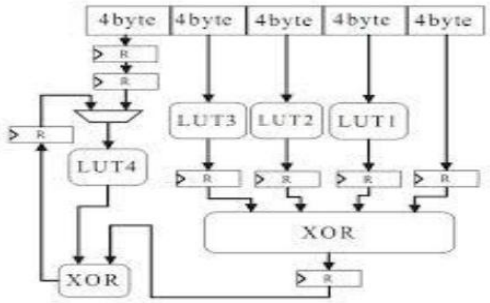

Fig.4.Fast CRC Update Architecture

Our fast CRC update method is extended from the parallel CRC calculation and can adapt to a number of bits processed in parallel. The method can also reduce the data traffic and power consumption of the CRC calculation unit.

(b) LFSR in CRC:

In traditional hardware implementations, a simple circuit based on shift registers performs the CRC calculation by handling the message one bit at a time. A typical serial CRC using LFSRs is it illustrates one possible structure for CRC32. There are a total of 32 registers the middle ones are left out for brevity. The combinational logic operation in the figure is the XOR operation. One bit is shifted in at each clock pulse. This circuit operates in a fashion similar to manual long division. The XOR gates hold the coefficients of the divisor corresponding to the indicated powers of x. Although the shift register approach to computing CRCs is usually implemented in hardware, this algorithm can also be used in software when bit-by-bit

processing is adequate.

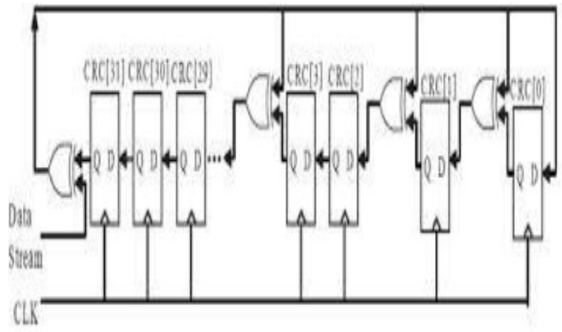

Fig.5.Serial CRC circuit using LFSRs

The proposed design starts from LFSR, which is generally used for serial CRC. An unfolding algorithm is used to realize parallel processing. However, direct application of unfolding may lead to a parallel CRC circuit with long iteration bound, which is the lowest achievable CP.

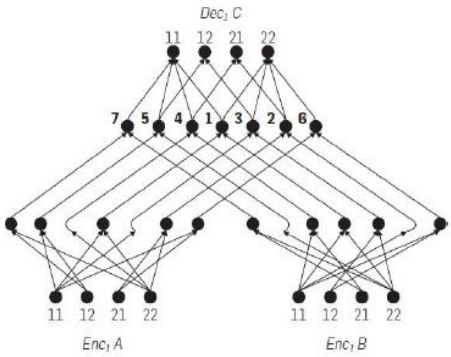

Fig.6.F-matrix algorithm

Two novel look-ahead pipelining methods are developed to reduce the iteration bound of the original serial LFSR CRC structures; then, the unfolding algorithm is applied to obtain a parallel CRC structure with low iteration bound. The retiming algorithm is then applied to obtain the achievable lowest CP.

Parallelly data input is processed; it is ANDed with the F-matrix generation from the generated polynomial. Result of that will XORed with present state CRC checksum. The final result will obtained after (k+m)/w cycles. Generation of F-matrix: F-matrix generated from the generated polynomial, matrix form can be represented as:

$$F = \begin{bmatrix} P_{m-1} & 1 & 0 & 0 & 0 \\ P_{m-2} & 0 & 1 & 0 & 0 \\ P_{m-3} & 0 & 0 & 1 & 0 \\ P_{m-4} & 0 & 0 & 0 & 1 \\ .. & .. & .. & .. & .. \\ P_0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Where {p0……pm-1} is generator polynomial. For example, the generator polynomial for CRC4 is {1, 0, 0, 1, and 1} and w-bits are parallel processed.

$$F = \begin{bmatrix} 1 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \end{bmatrix} \qquad F^4 = \begin{bmatrix} 0 & 1 & 1 & 1 \\ 1 & 1 & 0 & 0 \\ 1 & 1 & 1 & 0 \\ 1 & 1 & 1 & 1 \end{bmatrix}$$

Where {p0……pm-1} is generator polynomial. For example, the generator polynomial for CRC4 is {1, 0, 0, 1, and 1} and w-bits are parallel processed.

Here w=m=4, for that matrix calculated as follow. Parallel architecture: Parallel architecture based on F-matrix"d" is data that is parallel processed (i.e. 32bit), 'X is next state, X is current state(generated CRC), F (i) (j) is the ith row and jth column of FW matrix. If X = [xm1 …..x1 x0]T is utilized to denote the state of the shift registers, in linear system theory, the state equation for LFSRs can be expressed in modular 2 arithmetic as follow. Xi´= (P0⊗ Xm-1)⊕d Where, X(i) represents the state of the registers, X(i + 1) denotes the state of the registers, d denotes the one bit shift-in serial input. F is an m x m matrix and G is a 1 x m matrix. G = [0 0 --------0 1] T. the final representationX'=Fw⊗X⊗d.

If W-bits are parallel processed, the result of the CRC will generated after (k+m)/w cycles.

IV- EXPERIMENT RESULTS

Each architecture is coded in Verilog and simulated. The simulation results and the net List simulation are verified for each architecture. For the message bits: 11010011101100 And for the generator polynomial 1+Y+Y2+Y3 i.e., 1011.

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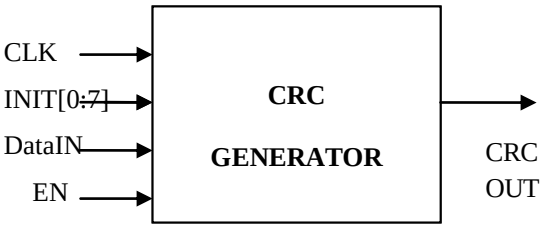
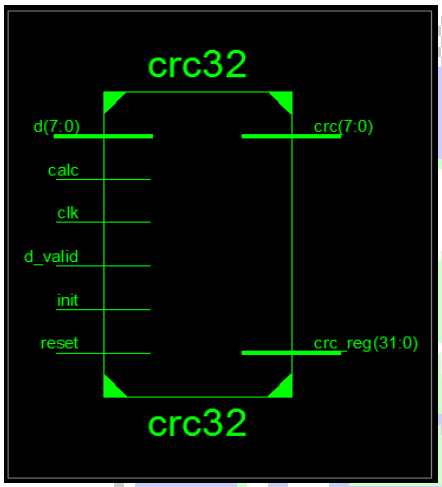
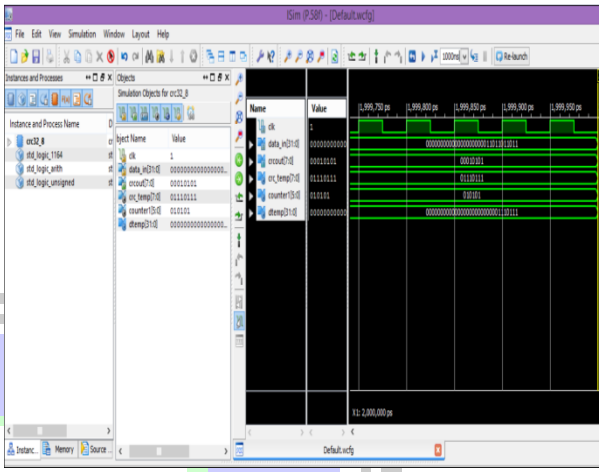
(a) Black Box View







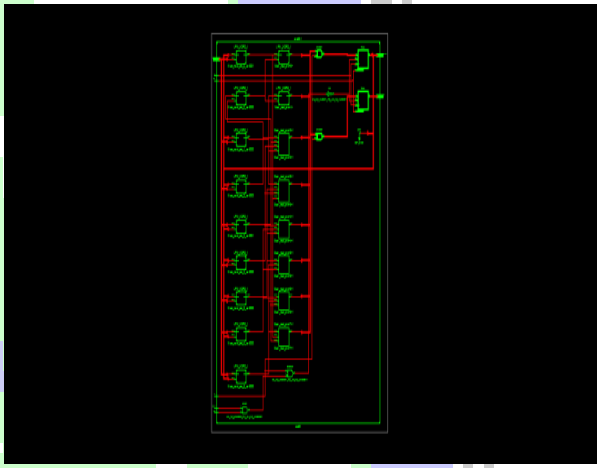
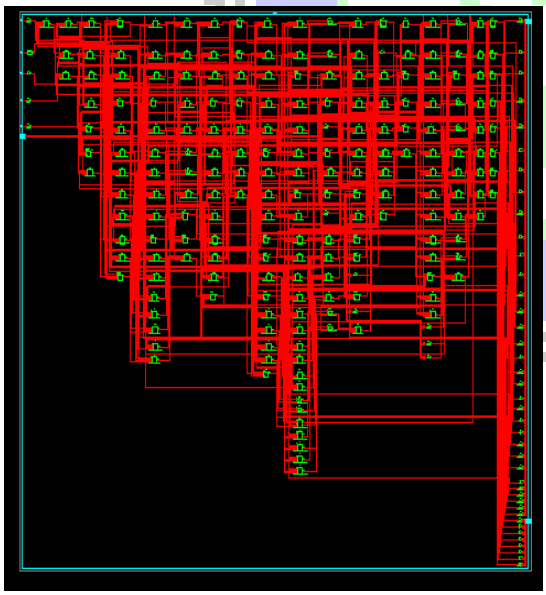
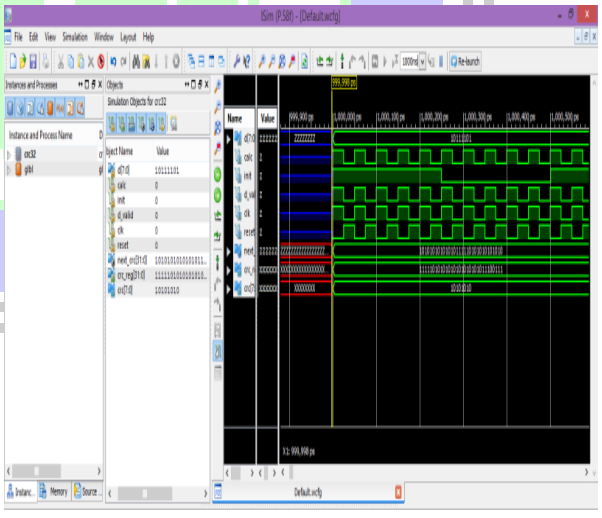


Fig.7.Black Box View

(b) Simulation Results:





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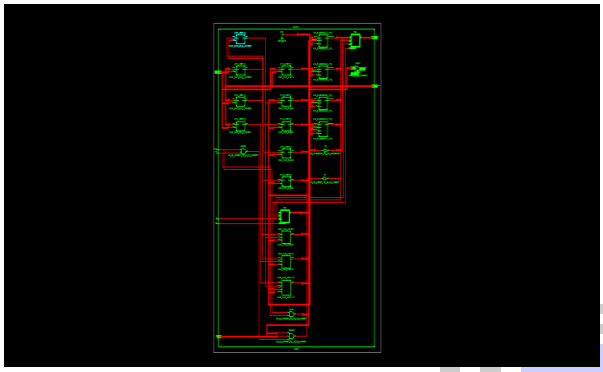

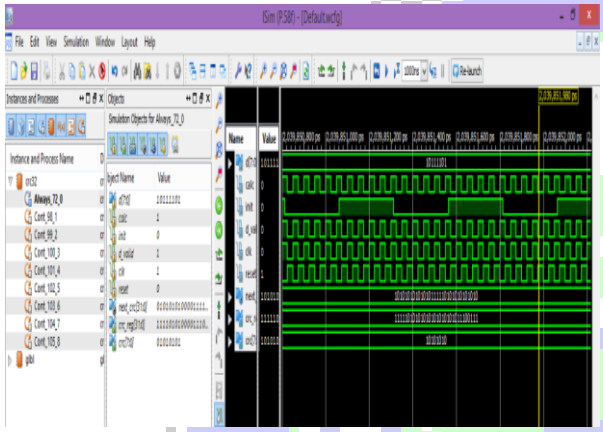

Fig.8.Simulation Results

(c) Table: Schematic, timing report, hardware resources

Device utilization summary	TIMING REPORT	HDL Synthesis Report
Selected Device : 3s50pq208-5	clk | BUFGP | 43	# Registers : 43
Number of Slices: 76 out of 768 9%	Speed Grade: -5	Flip-Flops : 43
Number of Slice Flip Flops: 43 out of 1536 2%	Delay: 5.047ns (Levels of Logic = 3)	Design Statistics # IOs : 53
Number of 4 input LUTs: 142 out of 1536 9%	Clock period: 5.047ns (frequency: 198.151MHz)	# BELS : 156
Number of IOs: 53	Total number of paths / destination ports: 274 / 43	# FlipFlops/Latches : 43
Number of bonded IOBs: 53 out of 124 42%	Total 5.047ns (2.239ns logic, 2.808ns route) (44.4% logic, 55.6% route)	FDPE : 43
Number of GCLKs: 1 out of 8 12%	Offset: 6.633ns	Clock Buffers : 1 # BUFGP : 1 # IO Buffers : 52 # IBUF : 12 # OBUF : 40

V-CONCLUSION

Generally when high-speed data transmission is required serial implementation is not preferred because of slow throughput. So parallel implementation is preferred which takes less time. CRC-32 requires 17 clock cycles to transmit 64bytes of data. But CRC-64 needs 9 clock cycles to transmit the same data. So, it drastically reduces computation time to 50% and same time increases the throughput.

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