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POWER AND LATENCY OPTIMIZED PRPG FOR BIST APPLICATIONS

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ABSTRACTS:

This project presents a Test vectors generation and can either yield a desired fault coverage faster than the conventional pseudorandom patterns while still reducing toggling rates down to desired levels. This project presents very attractive LP test scheme that allows for trading-off test coverage, pattern counts, and toggling rates in a very flexible manner. This project presents a Test vectors generation and can either yield desired fault coverage faster than the conventional pseudorandom patterns while still reducing toggling rates down to desired levels. Further this technique is enhanced with scan chain re ordering technique for further improving the power. Scan chain reordering means, reordering the inputs in such a way that the number of transitions in input and output is very less.

KEYWORDS: Test vector, Linear feedback shift Register (LFSR), Bit swapping, Scan chain reordering

INTRODUCTION: The semiconductor technology, design characteristics, and the design process are among the key factors that will impact this evolution. With new types of defects that one will have to consider to provide the desired test quality for the next technology nodes such as 3-D, it is appropriate to pose the question of what matching design-for-test (DFT) methods will need to be deployed. Test compression, introduced a decade ago, has quickly become the main stream DFT methodology. However, it is unclear whether test compression will be capable of coping with the rapid rate of technological changes over the next decade.

Interestingly, logic built-in self-test (LBIST), originally developed for board, system, and in-field test, is now gaining acceptance for production test as it provides very robust DFT and is used increasingly often with test compression. Running the test at a slower frequency than in normal mode. This technique of reducing power consumption, while easy to implement, significantly increases the test application time. Reduce the power consumption in scan-based built-in self-tests (BISTs) is by using scan chain-ordering techniques. These techniques aim to reduce the average-power consumption when scanning in test vectors and scanning out captured

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responses. Although these algorithms aim to reduce average-power consumption, they can reduce the peak power that may occur in the CUT during the scanning cycles, but not the capture power that may result during the test cycle (i.e., between launch and capture). However, it is unclear whether test compression will be capable of coping with the rapid rate of technological changes over the next decade

- Modifying the test vectors generated by the LFSR to get test vectors with a low number of transitions. The main drawback of these techniques is, it results in lower fault coverage and higher test application time.

Numerous schemes for power reduction during scan testing have been devised [14]. Among them, there are solutions specifically proposed for BIST to keep the average and peak power below a given threshold. For example, the test power can be reduced by preventing transitions at memory elements from propagating to combinational logic during scan shift. This is achieved by inserting gating logic between scan cell outputs and logic they drive [9], [19]. During normal operations and capture, this logic remains transparent. Gated scan cells are also proposed in [3] and [56]. A synergistic test power reduction method of [57] uses available on-chip clock gating circuitry to selectively block scan chains while employing test scheduling and planning to further decrease BIST power in the Cell processor. A test vector inhibiting scheme of [11] masks test patterns generated by an LFSR as not all produced vectors, often very lengthy, detect faults. Elimination of such tests can reduce switching activity with no impact on fault coverage. The advent of low-transition test pattern generators has added a new dimension to power aware BIST solutions [5], [32], [42]. For example, a device presented in [49] employs an LFSR to feed scan chains through biasing logic and

T-type flip-flop. Since this flip-flop holds the previous value until its input is asserted, the same value is repeatedly scanned into scan chains until the value at the output of biasing logic (e.g., a *k*-input AND gate) becomes 1. Depending on *k*, one can significantly reduce the number of transitions occurring at the scan chain inputs. A dual-speed LFSR of [48] consists of two LFSRs driven by normal and slow clocks, respectively. The switching activity is reduced at the circuit inputs connected to the slow-speed LFSR, while the whole scheme still ensures satisfactory fault coverage. Mask patterns mitigate the switching activity in LFSR-produced patterns as shown in [41], whereas a bit swapping of [1] achieves the same goal at the primary inputs of CUT. A gated LFSR clock of [12] allows activating only half of LFSR stages at a time. It cuts power consumption as only half of the circuit inputs change every cycle. Combining the low transition generator of [49] (handling easy-to-detect faults) with a 3-weight pseudorandom test pattern generator (PRPG) (detecting random pattern resistant faults) can also reduce BIST switching activity, as demonstrated in

Bit swapping LFSR : The bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions**.** The proposed BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells;

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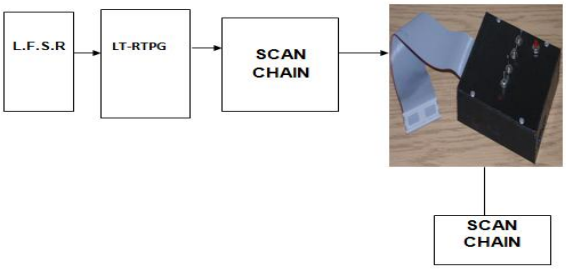
hence, the probabilities of having a 0 or 1 at a certain cell of the scan chain before applying the test vectors are equal. Hence, the proposed design retains an important feature of any random TPG. In the BS-LFSR, consider the case that $c1$ will be swapped with $c2$ and $c3$ with $c4, \ldots, cn-2$ with $cn-1$ according to the value of cnwhich is connected to the selection line of the multiplexers. In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced.

BIST BIST is a viable approach to test today's digital systems. With the ever increasing need for system integration, the trend today is to include in the same VLSI device a large number of functional blocks, and to package such devices, often, in Multi-Chip Modules (MCMs) that comprise complex systems. This leads to difficult testing problems in the manufacturing process and in the field**.** An attractive approach to solve these problems is to use a multi-level integrated Built-In Self-Test (BIST) strategy**.** This strategy assumes that BIST is used at each level of manufacturing test, and it is reused at all consecutive levels, i.e. device, MCM, board, system. Boundary-Scan standard to realize self-testing at different levels. This strategy can only be realized



These patterns are applied to CUT and the outputs generated from CUT are again stored in scan chain. For every input response stored in scan chain the corresponding output patterns are stored in the scan chain i.e., located at the output of the CUT. Here in comparator, it compares the input to CUT and corresponding output of CUT. And here if there is a difference obtained at the output of the comparator fault will be detected, else there is no fault in the circuit. Here more hardware overhead is implemented, Due to this structure more number of transitions occurred and hence more power is consumed. In order to reduce the power consumption with high efficiency we need to include extra circuitry. As with all applications, we may encounter various error messages if something goes wrong with the script or if we have made a mistake handling the application. I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing).Real defects (often mechanical) too numerous and often not analyzable

BIT-SWAPPING L.F.S.R

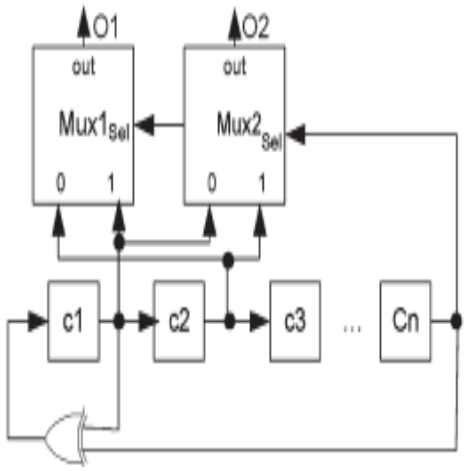


FIG: external L.F.S.R with bit-swapping

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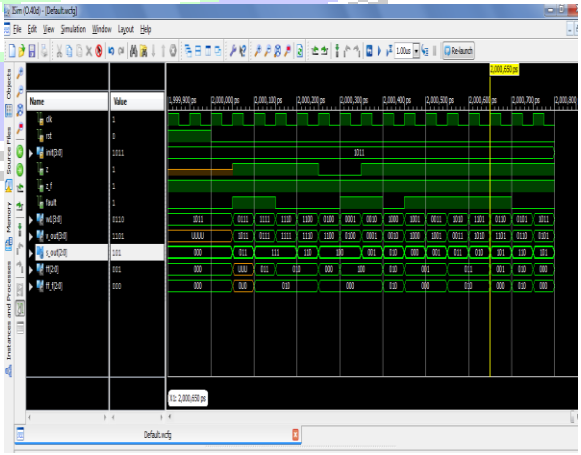
The above figure shows the external LFSR by using bit swapping technique. Bit swapping is a swap of a bit from 'm' position to tone 'n' position. It is used to reduce the transitions occurred at the input side of applying test vectors to circuit. The proposed BS-LFSR reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transitions in the scan input of the CUT. So from the above circuitry we can reduce the peak power while applying the test vectors to the circuitry. By reducing the number of transitions in the L.F.S.R we are going to reduce the peak power. In this section we are applying SCAN CHAIN ORDERING algorithm. In this scan-chain-ordering algorithm, some cells of the ordered scan chain will be reordered again in order to reduce the peak power which may result during the test cycle. This phase mainly depends on an important property of the BS-LFSR. This property states that, if two cells are connected with each other, then the probability that they have the same value at any clock cycle is 0.75 So in this project, while capturing the responses, we are reducing both average power and peak power.

- The proposed BS-LFSR has been combined with a cell-ordering algorithm, that reduces the number of transitions in the scan chain while scanning out the captured response.
- The problem of the capture power (peak power in the test cycle) will be solved by using a novel algorithm that will reorder some cells in the scan chain in such a way that minimizes the Hamming distance between the applied test vector and the captured response in the test cycle, hence reducing the test cycle peak power (capture power).

In recent years, the design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. As a consequence, many techniques have been introduced to minimize the power consumption of new VLSI systems. However, most of these methods focus on the power consumption during normal mode operation, while test mode operation has not normally been a predominant concern.

However, it has been found that the power consumed during test mode operation is often much higher than during normal mode operation. This is because most of the consumed power results from the switching activity in the nodes of the circuit under test (CUT), which is much higher during test mode than during normal mode operation. A direct technique to reduce power consumption is by running the test at a slower frequency than that in normal mode. This technique of reducing power consumption, while easy to implement, significantly increases the test application time. Furthermore, it fails in reducing peak-power consumption since it is independent of clock frequency.

RESULT:



CONCLUSION: A low-transition TPG that is based on some observations about transition counts at the output sequence of LFSRs has been presented. The proposed TPG is used to generate test vectors for test-per scan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented. When the BS-LFSR is used together with the proposed scan-chain-ordering algorithm, the average and peak powers are substantially reduced. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between the proposed design and other previously published methods show that the proposed design can achieve better results for most tested benchmark circuits.

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