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INPUT VECTOR MONITORING CONCURRENT BIST ARCHITETURE USING SRAM CELLS

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ABSTRACT

From all these years of VLSI design, it has been identified that the power consumed during the test mode operation is generally high compared to the normal mode operation. The switching activity in the nodes of the circuit under test (CUT) explains this high power dissipation in the test mode. This project presents test vector generation by proposing a Bit swapping LFSR that is based upon some new observations concerning the number of transitions produced at the output of an LFSR. The BS-LFSR reduces the number of transitions occurring at the scan-chain input during scan shift operation by 25%, compared to the normal LFSR, specially for the case of scan-based built-in self-tests. Thus the overall switching activity and hence the power dissipated in the circuit under test is reduced. The BS-LFSR is further combined with a Scan-chain Re-ordering algorithm that orders the cells in such a way so as to reduce the average and peak power (scan and capture) while scanning out a response to a signature analyzer. These techniques have a remarkable effect on the average- and peak-power reductions with negligible effect on the fault coverage or test application time.

KEYWORDS : Linear feedback shift Register (LFSR), Low Transition /random Test Pattern Generator (LT-RTPG), Bit swapping, Scan Chain re-Ordering (SCO

INTRODUCTION

The semiconductor technology, design characteristics, and the design process are among the key factors that will impact the development of the VLSI technology. With new types of defects that one will have to consider to provide the desired test quality for the next technology nodes such as 3-D, it is appropriate to pose the question of what matching design-for-test (DFT) methods will need to be deployed. Test compression, introduced a decade ago, has quickly become the main stream DFT methodology. However, it is unclear whether test compression will be capable of coping with the rapid rate of technological changes over the next decade. Interestingly, logic built-in self-test (LBIST), originally developed for board, system, and in-field test, is now gaining acceptance for production test as it provides very robust DFT and is used increasingly often with test compression. Running the test at a slower frequency than in normal mode is another option. This technique of reducing power

consumption, while easy to implement, significantly increases the test application time.

The power consumption in scan-based built-in self-tests (BISTs) can be reduced by using scan chain-ordering techniques. These techniques aim to reduce the average-power consumption when scanning in test vectors and scanning out captured responses. Although these algorithms aim to reduce average-power consumption, they can reduce the peak power that may occur in the CUT during the scanning cycles, but not the capture power that may result during the test cycle (i.e., between launch and capture). Modifying the test vectors generated by the LFSR to get test vectors with a low number of transitions. The main drawback of these techniques is, it results in lower fault coverage and higher test application time.

Numerous schemes for power reduction during scan testing have been devised. Among them, there are solutions specifically proposed for BIST to keep the average and peak power below a given threshold. For example, the test power can be reduced by preventing transitions at memory elements from propagating to combinational logic during scan shift. This is achieved by inserting gating logic between scan cell outputs and the logic they drive [9]. During normal operations and capture, this logic remains transparent. Gated scan cells have also been proposed [3]. Another synergistic test power reduction method uses available on-chip clock gating circuitry to selectively block scan chains while employing test scheduling and planning to further decrease BIST power in the Cell processor. A test vector inhibiting scheme masks test patterns generated by an LFSR as not all produced vectors, often very lengthy, detect faults. Elimination of such tests can reduce switching activity with no impact on fault coverage. The advent of low-transition test pattern generators has added a new dimension to power aware BIST solutions [5]. For example, devices presented in previous research employs an LFSR to feed scan chains through biasing logic and T-type flip-flop. Since this flip-flop holds the previous value until its input is asserted, the same value is repeatedly scanned into scan chains until the value at the output of biasing logic (e.g., a *k*-input AND gate) becomes 1. Depending on *k*, one can significantly reduce the number of transitions occurring at the scan chain inputs. Another option is using a dual-speed LFSR consisting of two LFSRs driven by normal and slow clocks, respectively. The switching activity is reduced at the circuit inputs connected to the slow-speed LFSR, while the whole scheme still ensures satisfactory fault coverage. Mask patterns mitigate the switching activity in LFSR-produced patterns, whereas a bit swapping of [1] achieves the same goal at the primary inputs of CUT. A gated LFSR clock allows activating only half of LFSR stages at a time. It cuts power consumption as only half of the circuit inputs change every cycle. Combining the low transition generator (handling easy-to-detect faults) with a 3-weight pseudorandom test pattern generator (PRPG) (detecting random pattern resistant faults) can also reduce BIST switching activity.

BIST

BIST is a viable approach to test today's digital systems. With the ever increasing need for system integration, the trend today is to include in the same VLSI device a large number of functional blocks, and to package such devices, often, in Multi-Chip Modules (MCMs) that comprise complex systems. This leads to difficult testing problems in the manufacturing process and in the field**.** An attractive approach to solve these problems is to use a multi-level integrated Built-In Self-Test (BIST) strategy**.** This strategy assumes that BIST is used at each level of manufacturing test, and it is reused at all consecutive levels, i.e. device, MCM, board, system. Boundary-Scan standard to realize self-testing at different levels.

Built In Self Test (BIST) provides a built in capability that would allow a circuit to be self testable. The purpose of BIST is to implement the function of Automatic Test Equipment (ATE) on the CUT. In BIST, the generated test patterns are applied to the circuit-under-test (CUT) with the help of on-chip hardware, and thus minimizing hardware overhead is a major concern of BIST implementation.

Bit swapping LFSR

The bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions**.** The proposed BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells; hence, the probabilities of having a 0 or 1 at a certain cell of the scan chain before applying the test vectors are equal. Hence, the proposed design retains an important feature of any random TPG. In the BS-LFSR, consider the case that $c1$ will be swapped with $c2$ and $c3$ with $c4, \ldots,$ $cn-2$ with $cn-1$ according to the value of cn which is connected to the selection line of the multiplexers. In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced.

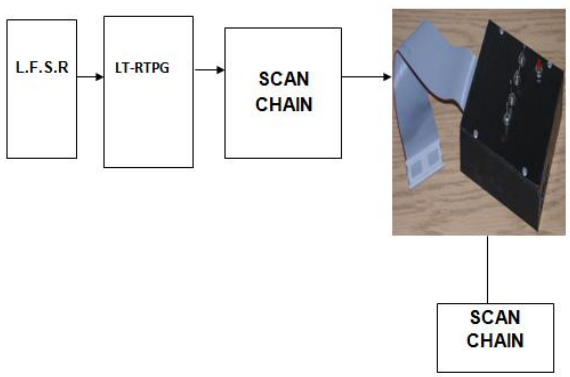


Fig 1: Bit Swapping LFSR

These patterns are applied to CUT and the outputs generated from CUT are again stored in scan chain. For every input response stored in scan chain the corresponding output patterns are stored in the scan chain i.e., located at the output of the CUT. Here in comparator, it compares the input to CUT and corresponding output of CUT. And here if there is a difference obtained at the output of the comparator fault will be detected, else there is no fault in the circuit. Here more hardware overhead is implemented, due to this structure more number of transitions occurred and hence more power is consumed. In order to reduce the power consumption with high efficiency we need to include extra circuitry. As with all applications, we may encounter

various error messages if something goes wrong with the script or if we have made a mistake handling the application. I/O function tests inadequate for manufacturing (functionality versus component and interconnect testing). Real defects (often mechanical) are too numerous and often not analyzable.

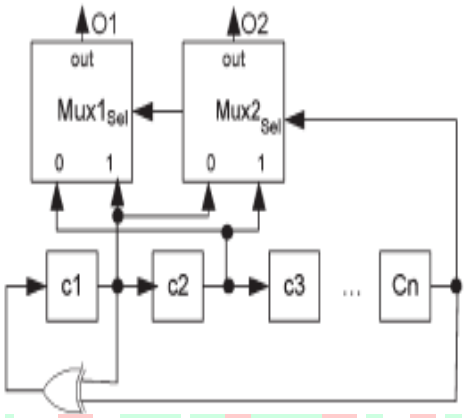


Fig 2: External L.F.S.R with bit-swapping

The above figure shows the external LFSR by using bit swapping technique. Bit swapping is a swap of a bit from 'm' position to tone 'n' position. It is used to reduce the transitions occurred at the input side of applying test vectors to circuit. The proposed BS-LFSR reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transitions in the scan input of the CUT. So from the above circuitry we can reduce the peak power while applying the test vectors to the circuitry. By reducing the number of transitions in the L.F.S.R we are going to reduce the peak power.

SCAN CHAIN RE-ORDERING (SCO)

Scan chain is a technique used in Design for Testing (DFT). The objective of a scan chain is to make testing easier by providing a simple way to set and observe each and every flip-flop (cell) in an IC. The basic structure of a scan includes :

- Scan_in and scan_out signals that define the input and output of a scan chain
- A scan enable pin is a special signal that is added to a design.
- A clock signal, which is used for controlling all the FFs in the chain during shift phase and the capture phase

The problem of excessive power during test is much more severe during scan testing as each test pattern require a large number of shift operations that contribute to unnecessarily increase the switching activity.

In this section we are applying Scan Chain Re-Ordering (SCO) algorithm. The basic idea of a scan chain re-order is to :

- Reduce the # of 0-1 shifting in scan cells
- Reduce wire length of the scan chain
- Thus the power consumption is reduced

In this scan-chain-ordering algorithm, some cells of the ordered scan chain will be reordered again in order to reduce the peak power which may result during the test cycle. This phase mainly depends on an important property of the BS-LFSR. This property states that, if two cells are connected with each other, then the probability that they have the same value at any clock cycle is 0.75 So in this

project, while capturing the responses, we are reducing both average power and peak power.

- The proposed BS-LFSR has been combined with a cell-ordering algorithm, that reduces the number of transitions in the scan chain while scanning out the captured response.
- The problem of the capture power (peak power in the test cycle) will be solved by using a novel algorithm that will reorder some cells in the scan chain in such a way that minimizes the Hamming distance between the applied test vector and the captured response in the test cycle, hence reducing the test cycle peak power (capture power).

RESULT:

It has been proved that the overall power dissipation has been decreased when the proposed Bitswapping and scan chain re-ordering techniques have been implemented simultaneously on the S27 circuit. We have compared the theoretical and the practical circuits of the S27 IC and compared the results, depicting a fault when the output is a 1.

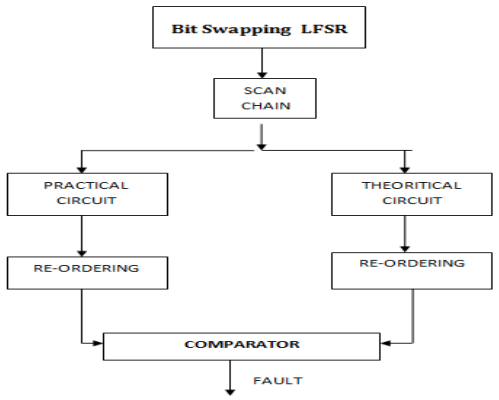
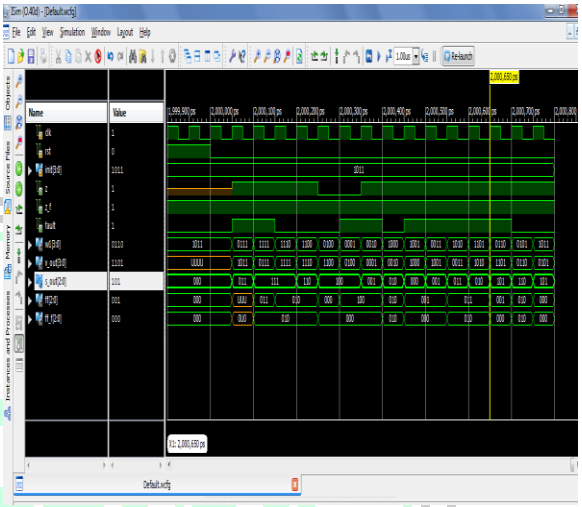
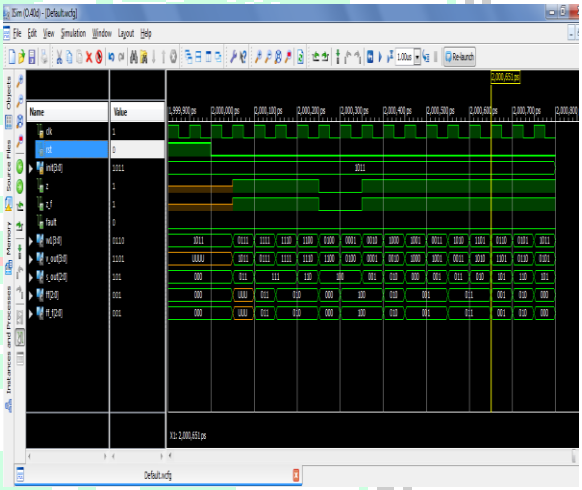


Fig 3: Block Diagram of Implementation of Scan Chain Re-ordering

ENHANCED ARCHITECTURE - WITH FAULTS



ENHANCED ARCHITECTURE - WITHOUT FAULTS



Compared with existing low power scan techniques, our solution offers numerous advantages. The proposed approach works for any conventional scan design - no extra DFT logic is required – and both the fault coverage and the overall test time are left unchanged. The power dissipation figures for the normal and the bit swapping LFSRs is as shown in the table 1.

LFSR	*Power*
Normal LFSR	***0.179***
Bit Swapping LFSR	***0.167***

Table 1: Power Dissipation

CONCLUSION

A low-transition TPG that is based on some observations about transition counts at the output sequence of LFSRs has been presented. The proposed TPG is used to generate test vectors for test-per scan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented. When the BS-LFSR is used together with the proposed scan-chain-ordering algorithm, the average and peak powers are substantially reduced. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between the proposed design and other previously published methods show that the proposed design can achieve better results for most tested benchmark circuits.

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