

Design of an Efficient Router in Networks

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ABSTRACT The main objective of the paper is to design an efficient router to transfer error free data between networks. The data is transferred in packet format and the length of each packet is 64 bytes. This Design consists of Register, FSM, Synchronizer and 3FIFO modules. The design have three output ports and one input port, it is a packet based Protocol. The Router drives the incoming packet from the input port to output port based on the address field contained in the packet Header. When parity mismatch exist between packet parity and internal parity then transfer of accurate data between networks is not possible. In this paper an error detection technique called parity checking is used. This technique tests the integrity of digital data being transmitted between server and client. This technique ensures that the data transmitted by the server can be received by the client network without getting corrupted. Packet routing, parity checking are the vital features of this efficient router. This design is synthesized and simulated in Xilinx ISE 13.1

Key Words: Router, Register, FSM, Synchronizer, FIFO, Parity mismatch, Error free data, Packet routing, Parity checking.

I INTRODUCTION

A router is a device that can forward data packets between computer networks. Routers perform the data "traffic direction" functions on the Internet. It can connect two or more data lines from different networks. When a data packet comes in one of these lines, the router reads the address information in the packet to determine its ultimate destination. Then, using the information in its packet header field, it directs the packet to the next network on its journey. The communication on network is carried out by means of a router, so the router should be efficiently designed. This router supports three parallel connections at the same time as we have three FIFO's. It uses store and forward type of flow control and FSM Controller to improve the performance of the router. The switching mechanism used here is packet switching. In packet switching the data is transferred in the form of packets between routers and independent routing decision is taken. In this router both input and output buffering is used so congestion can be avoided at both sides. This router has one input port from which the packet enters and has three output ports where the packet is driven out. Packet contains 3 parts: Header, Payload and Parity. Packet width is 8 bits and the length of the packet is in between 1 byte to 63 bytes. Packet header contains two fields DA and length. Destination Address (DA) of the packet is of 2 bits. The router drives the packet to respective ports based on the destination address of the packet. Each output port has 2-bit unique port address. If the destination address of the packet matches to a particular port

address, then router drives the packet to that output port. Length of the data is 6 bits. Length is measured in terms of bytes. Payload data should be in terms of bytes. Parity contains the security check of the packet. Parity is calculated over the Header and Payload bytes of the packet.

II LITERATURE SURVEY

The most commonly used routers are home routers and small office routers that simply pass data like email, web pages and videos between home computers and the Internet. An example of a router may be the Digital Subscriber Line (DSL) router or owner's cable, which connects to the Internet through an Internet Service Provider (ISP). Most sophisticated routers like enterprise routers connect large business networks and forward data at high speed along the optical fiber lines of the Internet. Even though routers are typically dedicated as hardware devices, now a day's use of software-based routers has grown rapidly. What defines a router is not its shape, color, size or manufacturer, but its job is routing data packets between computers. Cable modem, which routes data between a PC and an ISP, can be considered as a router.

Generally, a router could simply be one of two computers running the Windows 98 (or higher) operating system connected together using Internet Connection Sharing (ICS). In this scenario, the computer that is connected to Internet is acting as the router for the second computer to obtain its

Internet connection. Going a step up from ICS, a category of hardware routers are there, which are used to perform the same basic task as ICS, but with more features and functions. These are often called as broadband or Internet connection sharing routers. These routers allow sharing one Internet connection to multiple computers.

Broadband or ICS routers will look a bit different depending on the manufacturer or brand. But the wired routers are generally a small box-shaped hardware device with ports on the front or back into which each computer is plugged. These routers also have a port to plug in the broadband modem. These ports allow the router to rout the data packets between each of the computers. Depending on the type of modem and Internet connection, router with phone or fax machine ports are also available.

III ROUTER DESIGN PRINCIPLES AND PROTOCOLS

This document provides specifications for the Router design. Router drives the incoming packet from the input port to output ports depends on the address contained in the packet header. This router is a network router has a one input port from which the packet enters and three output ports where the packet is driven out. Packet contains 3 parts: Header, Payload and Parity. The width of the packet is 8 bits and the length of the packet can be between 1 byte to 63 bytes. Packet header contains two fields DA and length. Destination address (DA) of the packet is of 2 bits.

The router drives the packet to respective ports based on the destination address of the packet. Each output port contains 2bit unique port address. If the destination address of the packet matches the port address, then router drives the packet to the output port. Length of the data is 6 bits. Length is measured in terms of bytes. Payload data is in terms of bytes. Parity field contains the security check of the packet. It is calculated over the header and payload bytes of the packet. XOR operation are performed over the header and payload bytes of the packet. If the parity values of both internal parity and external parity are same, then no error is present in the data. If both the internal parity and external parity values are not equal then error signal is enabled. This router supports three parallel connections at the same time as it has 3 FIFOs. It uses store and forward type of flow control and FSMController which improves the performance of the router. In packet switching the data transfers in the form of packets between routers and independent routing decision has taken. In this router both input and output buffering is used so that congestion can be avoided at both sides.

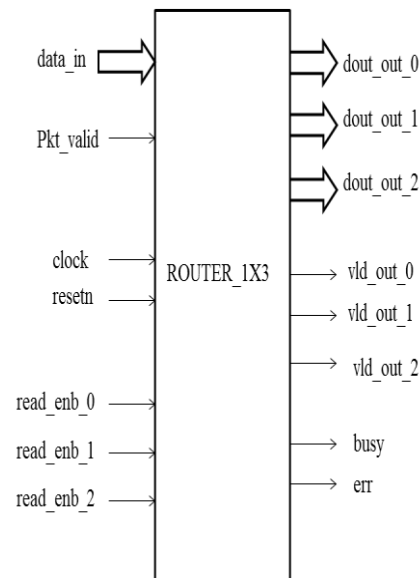


Figure 1: Router Top Level Block Diagram

IV ROUTER OPERATION

The three port router design is done by using of the four blocks. The blocks are Synchronizer, Register, Finite State Machine (FSM) and 3 FIFOs. Synchronizer module provides synchronization between router FSM and router FIFO modules. It provides faithful communication between single input port and three output ports. The register module has four internal registers in order to hold header byte, FIFO full state byte, internal parity and external parity. All the registers in this module are latched on the rising edge of the clock. The FSM module is the controller circuit for the router. This module generates all the control signals when a new packet is received by the router. These control signals are used by other design components in order to transfer the packet to the output port. There are three FIFOs used in the router design. Each FIFO is of 9 bits width and 16bytes depth. FIFO works on the system clock and is reset with a synchronous active low reset. The FIFO is also internally reset by an internal reset signal `soft_reset`. The FIFO memory size is 16X9. The extra bit in the data width is added in order to detect the header byte. `lfd_state` detects the header byte of a packet. The FIFOs store data packets and whenever the data is required to send that time the data will read from the FIFOs. In FIFO write operation takes place when FIFO is not full and read operation takes place when FIFO is not empty. The Router can operate with a single master device and one or more slave devices. If a single slave device is used, the `read_enb` (read enable) signal may be fixed to logic low if the slave permits it. With multiple slave devices, an independent `read_enb` signal is required from the master for each slave device.

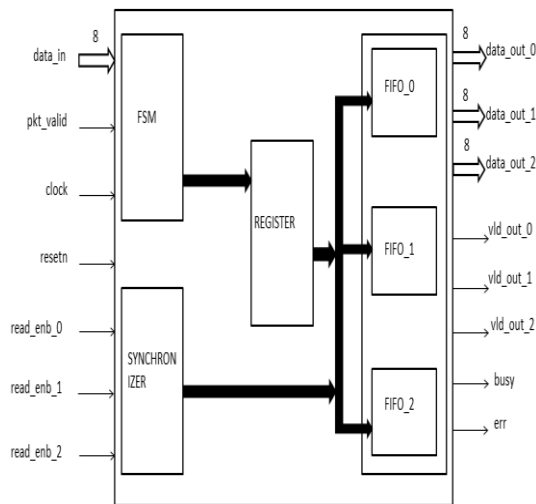


Figure 2: Router Internal Structure

V RESULTS

The code is implemented with Verilog language and is executed by XILINX ISE design suit (13.1 versions). Figure 3 shows simulation result of FSM module of the router. Signal `detect_add` is asserted when new incoming packet is detected. Signal `ldf_state` is asserted when the first data byte is loaded to the FIFO. Whenever the payload data is loading into the FIFO then Signal `ld_state` is asserted. When the data is loading into the FIFO then the `BUSY` signal is become low. Signal `write_enb_reg` is asserted in order to write the packet information (Header+ Payload+ Parity) to the selected FIFO.

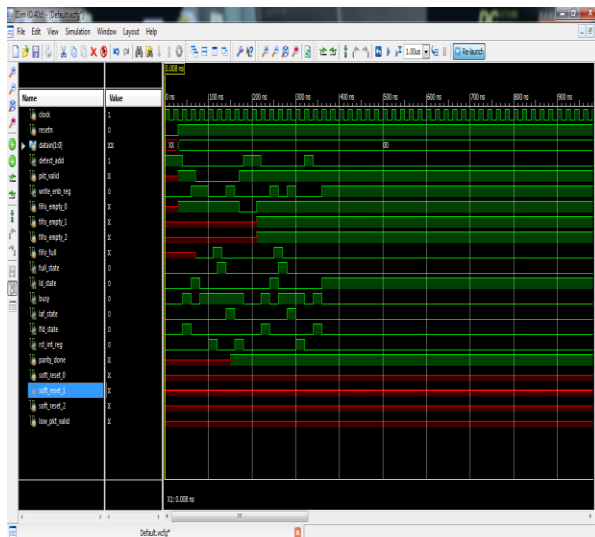


Figure 3: Simulation Resultsof FSM Module

Figure 4 shows the simulation result of FIFO module. Three FIFOs are used in the router design. In this result signal `data_in` is sampled at the rising edge of the clock when `write_enb` is high.

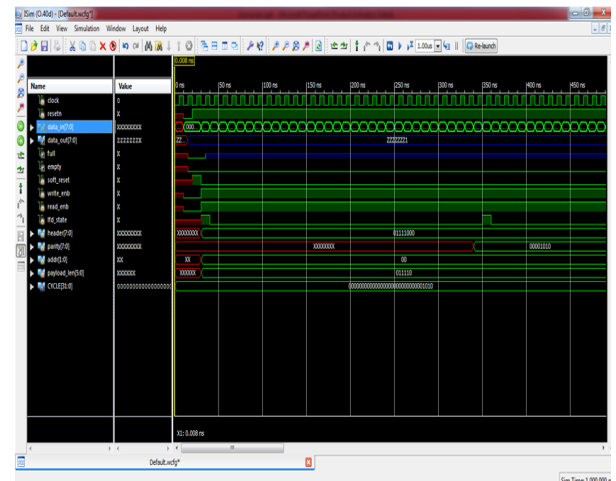


Figure 4:Simulation Results of FIFO Module

Figure 5 shows the simulation result of router top module. In the top module all the four modules are simulated. The `err` signal (error signal) will become high when it finds the mismatch between the packet parity and internal parity. `read_enb_0` become high when the packet is reading through output data bus `data_out_0`. Similarly `read_enb_1` and `read_enb_2`. `vld_out_0` signal will become high when a valid byte is available for destination client network 1. Similarly `vld_out_1` and `vld_out_2` signals also perform.

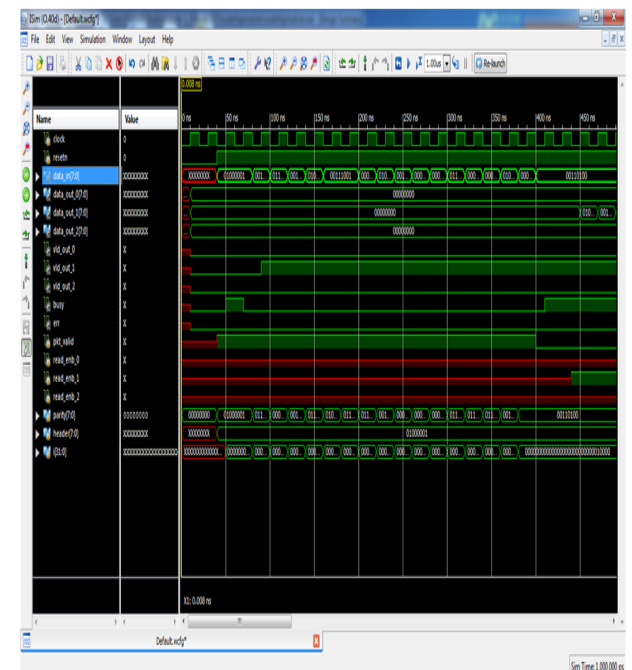


Figure 5: Simulation Results of Router Top Module

Synthesis Report:

Logic Utilization	Used	Available	Utilization Percentage
Number of Slices	602	960	62%
Number of 4 input LUT s	1138	1920	59%
Number of Bonded IOB s	43	108	39%
Number of GCLK s	1	24	4%

Table1: Device Utilization Summary of the Router

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VII CONCLUSION

Finally, this paper makes an attempt in presenting the design of an efficient router which forward data packets error freely between networks. The length of the packet is 64bits. This Router drives the incoming packet which comes from the input port to output ports based on the address contained in the packet header field. An error detection technique called parity checking is used to test the integrity of digital data being transmitted between server and client. This technique ensures that the data transmitted by the server network is received by the client network without getting corrupted. This will show error signal when mismatch exist between packet parity and internal parity of the data. By using this error detection technique the errors in the incoming data can be eliminated so that performance of the router can be improved.

As the future research, one can design a router having packet length of 128bytes. And can increase the number of client networks. As the packet length increases the numbers of client networks are increased. So this router can cater the needs of large business enterprises.

VI REFERENCES

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