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VOLTAGE SYNCHRONIZATION FOR DG SYSTEMS UNDER GRID FAULT CONDITIONS

Abdul Aleem[1],Sk.Shakir Hussain[2]

[1]M.Tech Student, Anu Bose Institute of Technology,Paloncha, khammam, Telangana, India

[2]Assoc Prof Dept of EEE, Anu Bose Institute of Technology,Paloncha, khammam, Telangana, India

Abstract— The genuine framework code necessities for the lattice association of disseminated era frameworks, primarily wind and photovoltaic (PV) frameworks, are turning out to be extremely requesting. The transmission framework administrators (TSOs) are particularly worried about the low-voltage-ride-through necessities. Arrangements in view of the establishment of STATCOMs and element voltage controllers (DVRs), and on cutting edge control functionalities for the current force converters of dispersed era plants, have added to upgrade their reaction under flawed and mutilated situations and, thus, to satisfy these necessities. Keeping in mind the end goal to accomplish tasteful results with such frameworks, it is important to rely on precise and quick network voltage synchronization calculations, which can work under uneven and bended conditions. This paper breaks down the synchronization ability of three propelled synchronization frameworks: the decoupled twofold synchronous reference outline stage bolted circle (PLL), the double second request summed up integrator PLL, and the three-stage improved PLL, intended to work under such conditions. Albeit different frameworks taking into account recurrence bolted circles have likewise been created, PLLs have been picked because of their connection withdq0 controllers. In the accompanying, the distinctive calculations will be introduced and discretized , and their execution will be tried in a trial setup controlled with a specific end goal to assess their precision and usage highlights.

INTRODUCTION

The power share of renewable energy-based generation systems is supposed to reach 20% by 2030, where wind and photovoltaic (PV) systems are assumed to be the most outstanding examples of integration of such systems in the electrical Manuscript received September 2, 2013; revised February 4, 2014 and April 12, 2014; accepted May 15, 2014. Date of publication January 13, 2015; date of current version July 15, 2015. Paper 2012-SECSC-582.R2, presented at the 2012 IEEE Energy Conversion Congress and Exposition, Raleigh, NC, USA, September 15–20, and approved for publication in the IEEE TRANSACTIONS ONINDUSTRY APPLICATIONS by the Sustainable Energy Conversion Systems Committee of the IEEE Industry Applications Society. This work was supported by the Spanish Ministry of Economy and Competitiveness under Project ENE2013-48428-C2-2-R.The increased penetration of these technologies in the electrical network has reinforced the already existing concern among the transmission system operators (TSOs) about their influence in the grid stability; as a consequence, the grid connection standards are becoming more and more restrictive for distribution generation systems in all countries. In the actual grid code requirements (GCRs), special constraints for the operation of such plants under grid voltage fault conditions have gained a great importance. These requirements determine the fault boundaries among those through which a grid-connected generation system shall remain connected to the network, giving rise to specific voltage profiles that specify the depth and clearance time of the voltage sags that they must withstand. Such requirements are known as low voltage ride through (LVRT) and are described by a voltage versus time characteristic . Although the LVRT requirements in the different standards are very different, as shown in [8], the first issue that generation systems must afford when a voltage sag occurs is the limitation of their transient response, in order to avoid its protective disconnection from the network. This is the case, for instance, of fixed speed wind turbines based on squirrel

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cage induction generators, where the voltage drop in the stator windings can conduct the generator to an overspeed tripping, as shown in . Likewise, variable speed wind power systems may lose controllability in the injection of active/reactive power due to the disconnection of the rotor side converter under such conditions.

1. GRID SYNCHRONIZATION SPECIFICATIONS BASED ON GCR

Even though several works are published within the field of grid synchronization, almost all of them are centered on analyzing the individual dynamic performance of each proposal, without first determining a time response window within the dynamic behavior of the system under test, which would be considered to be satisfactory. In this paper, in order to evaluate the response of the grid synchronization topologies under test, a common performance requirement for all the structures has been established in this section, considering the needs that can be derived from the LVRT requirements. Despite the fact that the detection of the fault can be carried out with simpler algorithms, as shown in [39] and , the importance of advanced grid synchronization systems lies in the necessity of having accurate information about the magnitude and phase of the grid voltage during the fault, in order to inject the reactive power required by the TSO. In the German standard [2], it is stated that voltage control must take place within 20 ms after the fault recognition, by providing a reactive current on the low voltage side of the. E-on voltage support requirement in the event of grid fault. REE voltage support requirement in the event of grid fault. Generator transformer to at least 2% of the rated current for each percent of the voltage dip, as shown in Fig. 1. 100% reactive power delivery must be possible, if necessary. A similar condition is given in the Spanish grid code, where the wind power plants are required to stop drawing inductive reactive power within 100 ms of a voltage drop and be able to inject full reactive power after 150 ms, Considering these demands, this paper will consider that the estimation of the voltage conditions will be carried out within 20–25 ms, as this target permits it to fulfill the most restrictive requirements, in terms of dynamical response, available in the grid codes. This condition will be extended to frequency estimation; although this parameter is more related to secondary control algorithms than LVRT, the same time window between 20 and 25 ms will be considered in this work for the detection of the disturbance.

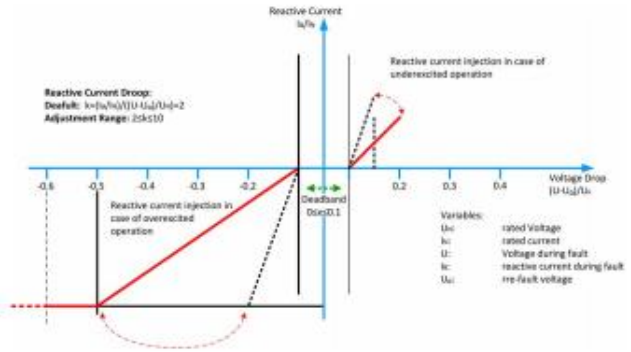
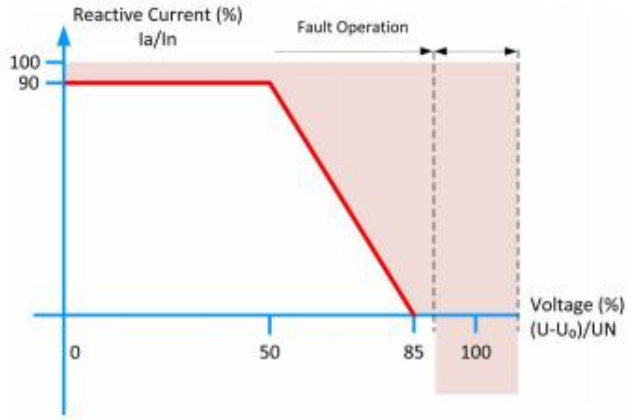


Fig. 1. E-on voltage support requirement in the event of grid fault.



A. DDSRF PLL

The DDSRF PLL, published in [34] and [41], was developed for improving the conventional SRF PLL. This synchronization system exploits two synchronous reference frames rotating at the fundamental utility frequency, one counterclockwise and another one clockwise, in order to achieve an accurate detection of the positive- and negative-sequence components of the grid voltage vector when it is affected by unbalanced grid faults. The diagram of the DDSRF PLL .When the three-phase grid voltage is unbalanced , the fundamental positive-sequence voltage vector

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appears as a dc voltage on the dq+1 axes of the positive-sequence SRF and as ac voltages at twice the fundamental utility frequency on the dq −1axes of the negative-sequence SRF. In contrast, the negative sequence voltage vector will cause a dc component on the negative-sequence SRF and an ac oscillation on the positive sequence SRF. Since the amplitude of the oscillation on the positive-sequence SRF matches the dc level on the negative sequence SRF and vice versa, a decoupling network is applied to signals on the dq positive/negative SRF axes in order to cancel out such ac oscillations. Low-pass filters (LPFs) are responsible for extracting the dc component from the signal on the decoupled SRF axes. These dc components collect information about the amplitude and phase angle of the positive- and negative-sequence components of the grid voltage vector. The decouple dq-axis signal of the positive-sequence SRF (v∗ q+1) and performs the same function as in an SRF PLL, aligning the positive-sequence voltage with thed-axis. This signal is free of ac components due to the effect of the decoupling networks; the bandwidth of the loop controller can be consequently increased.

B. DSOGI PLL

The operating principle of the DSOGI PLL for estimating the positive- and negative-sequence components of the grid voltage vectors is based on using the instantaneous symmetrical component (ISC) method on the αβ stationary reference frame, DSOGI-PLL block diagram. The diagram of the DSOGI PLL is shown As it can be noticed, the ISC method is implemented by the positive-sequence calculation block. To apply the ISC method, it is necessary to have a set of signals ,v αvβ, representing the input voltage vector on theαβ stationary reference frame together with another set of signals, qvα–qvβ, which are in quadrature and lagged with respect to vα–vβ. In the DSOGI PLL, the signals to be supplied to the ISC method are obtained by using a dual second order generalized integrator (DSOGI), which is an adaptive band pass filter based on the generalized integrator concept .

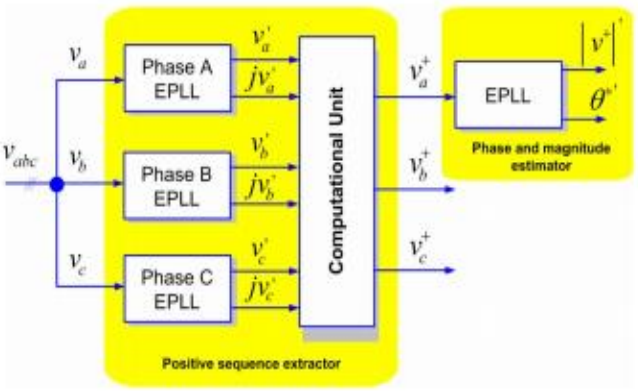
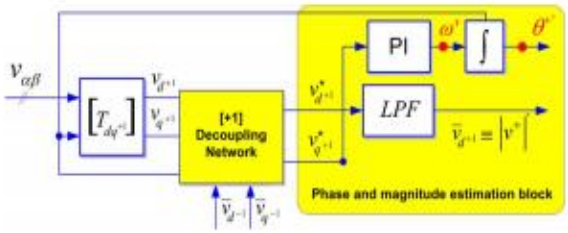


Fig. 5. 3phEPLL block diagram.



$$\begin{bmatrix} v^*_{d+1}[n+1] \\ v^*_{q+1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d+1}[n+1] \\ v_{q+1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(2\theta'[n]) & -\sin(2\theta'[n]) \\ \sin(2\theta'[n]) & -\cos(2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d-1}[n] \\ \bar{v}_{q-1}[n] \end{bmatrix} \times \begin{bmatrix} v^*_{d-1}[n+1] \\ v^*_{q-1}[n+1] \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{d-1}[n+1] \\ v_{q-1}[n+1] \end{bmatrix} + \begin{bmatrix} -\cos(-2\theta'[n]) & -\sin(-2\theta'[n]) \\ \sin(-2\theta'[n]) & -\cos(-2\theta'[n]) \end{bmatrix} \cdot \begin{bmatrix} \bar{v}_{d+1}[n] \\ \bar{v}_{q+1}[n] \end{bmatrix}.$$

The discrete controller and the integrator can be built using a backward numerical approximation. The frequency and phase can then be represented in the z-domain (2), considering ∗ q+1 as the error to be minimized. In this equation, a feed ;forward

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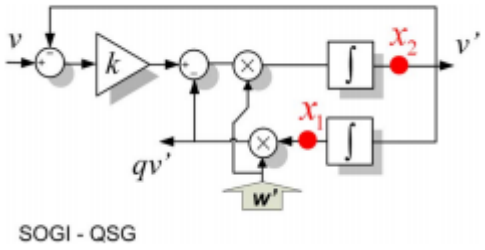
$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V^*_{q+1}(z) + \omega_{ff}$$
$$\theta^{+'} = \frac{T_s \cdot z}{z-1} \cdot W'(z). \quad (2)$$

Finally, sample-based representation gives rise to (3), which are the expressions to be implemented

$$\omega'[n+1] = \omega'[n] - k_p \cdot v^*_{q+1}[n] + (k_p + k_i \cdot T_s) \cdot v^*_{q+1}[n+1]$$
$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1]. \quad (3)$$

C. DSOGI-PLL Discretization

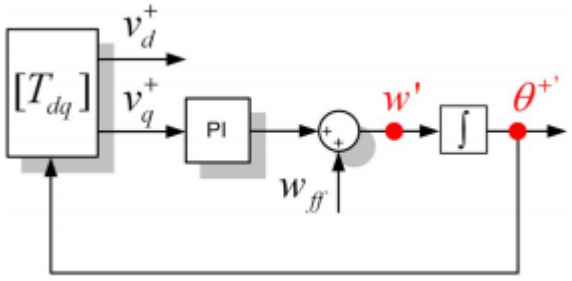
1) DSOGI-QSG Block Discretization: As was previously mentioned in Section II, the DSOGI-based quadrature signal generator (QSG) of Fig. 4 consists of two independent and decoupled second-order generalized integrators (SOGIs). Therefore, each SOGI-based quadrature signal generator can be discretized individually, thus facilitating its mathematical description. The block diagram of the implemented SOGI



SOGI - QSG

The discrete state space of (6) is obtained from the continuous representation by means of the mathematical procedure presented

$$A' = \left(I + \frac{A \cdot T_s}{2}\right)\left(I - \frac{A \cdot T_s}{2}\right)^{-1}$$
$$B' = \left(I - \frac{A \cdot T_s}{2}\right)^{-1} \cdot B$$
$$C' = T_s \cdot C \cdot \left(I - \frac{A \cdot T_s}{2}\right)^{-1}$$
$$D' = C \cdot \left(I - \frac{A \cdot T_s}{2}\right)^{-1} \cdot \frac{B \cdot T_s}{2}$$



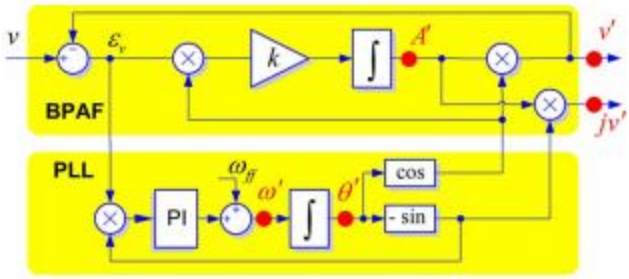
2) *SRF PLL Discretization:* The frequency and phase detection is obtained by means of the SRF PLL shown in Fig. 8. The discretization of the controller and the integrator is performed using the backward numerical approximation.

The frequency and phase can then be represented in the z-domain, as shown in (9), where v_q^+ constitutes the error to be minimized

$$W'(z) = \frac{(k_p + k_i \cdot T_s)z - k_p}{z-1} \cdot V^*_{q+1}(z) + \omega_{ff}$$
$$\theta^{+'} = \frac{T_s \cdot z}{z-1} \cdot W'(z). \quad (9)$$

It can be noticed that the previous equations in (9) are equal to (2), as, in both cases, an SRF PLL is implemented. Likewise, the sample-based representation of (9) can be written as shown in

$$\omega'[n+1] = \omega'[n] - k_p \cdot v^*_{q+1}[n] + (k_p + k_i \cdot T_s) \cdot v^*_{q+1}[n+1]$$
$$\theta^{+'}[n+1] = \theta^{+'}[n] + T_s \cdot \omega'[n+1]. \quad (10)$$



The fundamental componentizx 1in the circulating current can transport energy between the upper- and lower-arm capacitors .

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I. PROPOSED SYSTEM

According to this diagram, the state space representation of the EPLL in the continuous domain can be written as shown in

$$\dot{A}'(t) = k \cdot e(t) \cdot \cos\theta'(t)$$

$$\dot{\omega}'(t) = -k_i \cdot e(t) \cdot \sin\theta'(t)$$

$$\dot{\theta}(t) = \omega'(t) + \frac{k_p}{k_i} \cdot \dot{\omega}'(t). \qquad (11)$$

In packet switching the data transfers in the form of packets between cooperating routers and independent routing decision is taken. The store and forward flow mechanism is best because it does not reserve channels and thus does not lead to idle physical channels The arbiter is of rotating priority scheme so that every channel once get chance to transfer its data. In this router both input and output buffering is used so that congestion can be avoided at both sides. A router is a device that forwards data packets across computer networks. Routers perform the data “traffic direction" functions on the Internet.

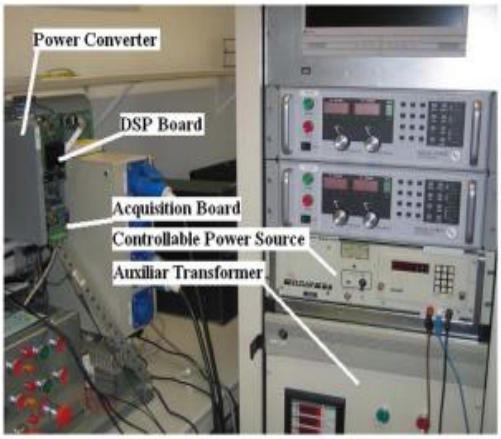
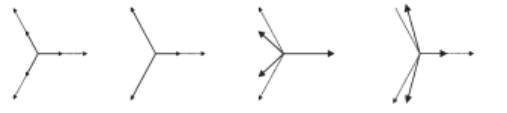


TABLE I
PROPERTIES OF THE TESTING VOLTAGE SAGS

A Sag	B Sag	C Sag	D Sag
$V^+ = 40\angle -40°$ $V^- = 0\angle 0°$ $V^0 = 0\angle 0°$	$V^+ = 73.3\angle -10°$ $V^- = 26.6\angle 170°$ $V^0 = 26.6\angle 170°$	$V^+ = 67.37\angle -5.7°$ $V^- = 27.81\angle 2.2°$ $V^0 = 0\angle 0°$	$V^+ = 67.37\angle -5.7°$ $V^- = 27.81\angle -177.8°$ $V^0 = 0\angle 0°$

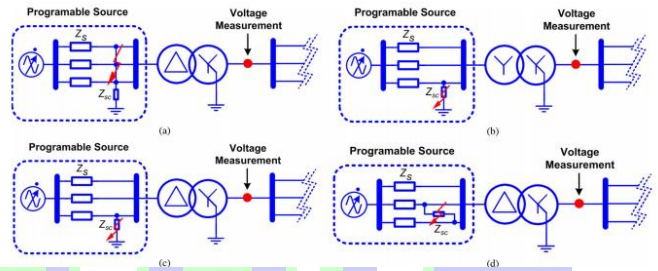


Positive, negative and homopolar sequence vectors during the fault conditions for the different sags

Thus communication is established between input and output ports. According to the destination path of data packet, control bit lines of FSM are set. The movement of data from source to destination is called Packet Switching. The packet switching mechanism is used here, in which the flit size is 8 bits .Thus the packet size varies from 0 bits to 8 bits.

B. Design of the Proposed Repetitive Controller

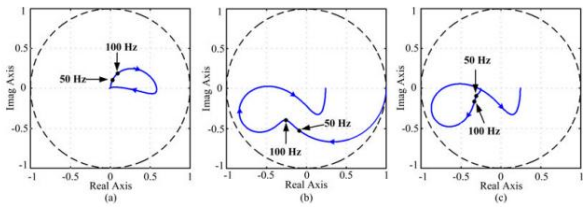
Fig. 6 is redrawn inz-domain and with more detail in Fig. 9, which shows the inner structure of the repetitive



$$i_{\mathrm{err}}(z) = \frac{[1 - P(z)][z^{N_s} - Q(z)]}{z^{N_s} - [Q(z) - K_r S(z) z^k P(z)]} i^*_{zx}(z)$$

$$- \frac{[1 - P(z)][z^{N_s} - Q(z)]}{z^{N_s} - [Q(z) - K_r S(z) z^k P(z)]} i_{zx\_k}(z). \qquad (10)$$

In the FIFO (First In First Out), the inputs are stored and forwarded. So this method is also called as store and forward technique.



The Cross Bar Switch is a MUX DEMUX network.It operates on the request signal granted by the Round Robin Network. For example, if the request signal is 10000 it enables the datouts line and transmits the data to the particular output line.

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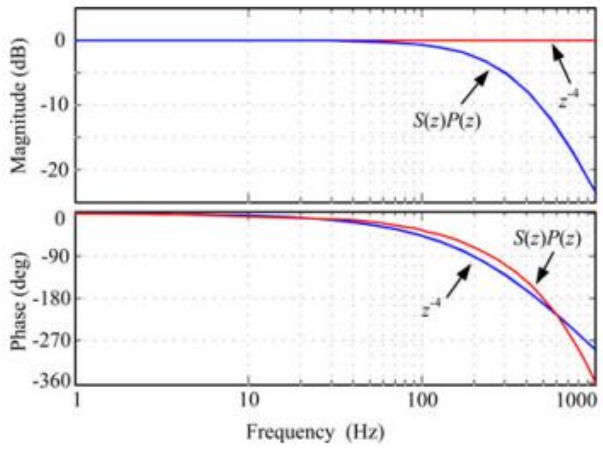

ţ. 10. Bode plot of $S(z)P(z)$ and z^{-k}.

CONCLUSION

This paper studied the behavior of three advanced grid synchronization systems. Their structures have been presented, and their discrete algorithms have been detailed. Moreover, their performances have been tested in an experimental setup, where these algorithms have been digitally implemented in a commercial DSP, allowing proof of their satisfactory response under balanced and distorted grid conditions. The DDSRF PLL and the DSOGI PLL allow estimating the ISCs of a three-phase system working in the αβreference frame, while the 3phEPLL uses the "abc" reference frame, thus working with three variables. As has been shown, this feature simplifies the structure of the DSOGI PLL and the DDSRF PLL, which allows reducing the computational burden, as compared to the 3phEPLL, without affecting its performance. The synchronization capability of the three PLLs under test has been shown to be fast and accurate under faulty scenarios, allowing the detection of the positive sequence of the voltage in 20–25 ms in all cases; however, the simpler structure of the DDSRF and the DSOGI affords an easier tuning of their control parameters and, therefore, a more accurate control of their transient response.

The immunity of the analyzed PLLs in the possibility of a polluted network is better when using the 3phEPLL and the DDSRF, due to their greater bandpass and low-pass filtering capabilities. Although the DSOGI also gives rise to reasonably good results, due to its inherent band pass filtering structure, its response is more affected by harmoni.

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