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Aging-Aware Reliable Multiplier Design with Adaptive Hold Logic

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ABSTRACT:

In VLSI, scaling methods plays an important role in reducing the power dissipation from one technology node to other technology node. The two major constraints for delay in any VLSI circuits are latency and throughput. The negative bias temperature instability (NBTI) effect occurs when a pMOS transistor is under negative bias (Vgs= -VDD) increasing the threshold voltage of pMOS transistor and reducing the speed. A similar phenomenon, positive bias temperature instability (PBTI) effect occurs when an nMOS transistor is under positive bias. These both effects degrade the transistor speed and system may fail due to timing violations. In this paper, an Adaptive Hold Logic (AHL) circuit is proposed to mitigate the performance degradation due to aging effects. The main objective of this project is to design an aging-aware variable-latency multiplier with the AHL. This project proposes an aging-aware multiplier design with novel adaptive hold logic (AHL) circuit. The multiplier is able to provide higher throughput through the variable latency and can adjust the AHL circuit to mitigate performance degradation that is due to the aging effect. Moreover, the proposed architecture can be applied to a column bypassing multiplier and enhanced using Baugh-wooley multiplication.

KEYWORDS: Aging, Positive Biasing, Negative Biasing, Temperature Instability, Column Bypass, Critical Path Delay, Razar flipflop.

INTRODUCTION: **D**IGITAL multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The throughput of these applications depends on multipliers, and if the multipliers are too slow, the performance of entire circuits will be reduced. Furthermore, negative bias temperature instability (NBTI) occurs when a pMOS transistor is under negative bias (Vgs = −Vdd). In this situation, the interaction between inversion layer holes and hydrogen-passivated Si atoms breaks the Si–H bond generated during the oxidation process, generating H or H2 molecules. When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface result in increased threshold voltage (Vth), reducing the circuit switching speed. When the biased voltage is removed, the reverse reaction occurs, reducing the NBTI effect. However, the reverse reaction does not eliminate all the interface traps generated during the stress phase, and Vth is increased in the long term. Hence, it is important to design a reliable high-performancemultiplier. The corresponding effect on an nMOS transistor is positive bias temperature instability (PBTI), which occurs when an nMOS transistor is under positive bias. Compared with the NBTI effect, the PBTI effect is much smaller on oxide/polygate transistors, and therefore is usually ignored. However, for high-k/metal-gate nMOS transistors with significant charge trapping, the PBTI effect can no longer be ignored. In fact, it has been shown that the PBTI effect is more significant than the NBTI effect on 32-nm high-k/metal-gate processes [2]–[4]. A traditional method to mitigate the aging effect is overdesign [5], [6], including such things as guard-banding and gate oversizing; however, this approach can be very pessimistic and area and power inefficient. To avoid this problem, many NBTI-aware methodologies have been proposed. An NBTI-aware technology mapping technique was proposed in [7] to guarantee the performance of the circuit during its lifetime. In [8], an NBTI-aware sleep transistor was designed to reduce the aging effects on pMOS sleep-transistors, and the lifetime stability of the power-gated circuits under consideration was improved. Wu and Marculescu [9] proposed a joint logic restructuring

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ISSUE-5
Page:7830-36

and pin reordering method, which is based on detecting functional symmetries and transistor stacking effects. They also proposed an NBTI optimization method that considered path sensitization [12].

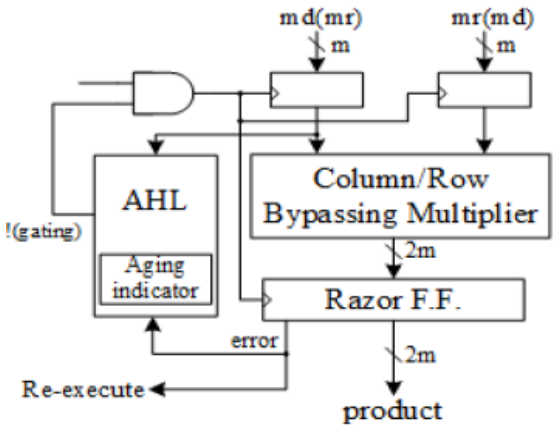
Aging Effects

Due to aggressive scaling of the device geometries and increasing electric fields, circuit aging has become an issue. Measurements on individual transistors were used to determine circuit design margins in order to guarantee reliability. Integrated-circuit aging phenomena observed in sub-90nm CMOS technologies are as follows [2]:-

1. Hot Carrier Injection (HCI).
2. Time-Dependent Dielectric Breakdown (TDDB).
3. Bias Temperature Instability (BTI).
4. Electro-migration (EM).

PROPOSED ARCHITECTURE:

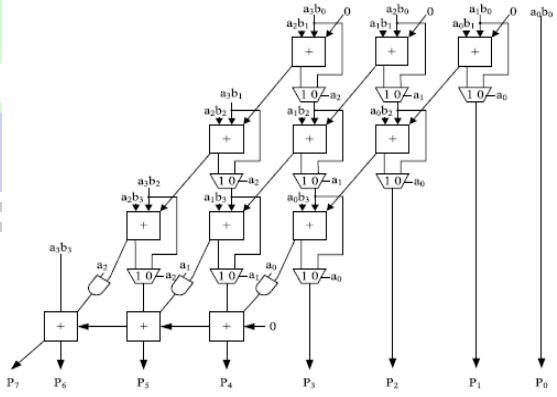
Below figure shows our proposed aging-aware multiplier architecture, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops [27], and an AHL circuit. The inputs of the row-bypassing multiplier are the symbols in the parentheses.In the proposed architecture, the column- and row-bypassingmultipliers can be examined by the number of zeros in either the multiplicand or multiplicator to predict whether the operation requires one cycle or two cycles to complete. When input patterns are random, the number of zeros and ones in the multiplicator and multiplicand follows a normal distribution



the two aging-aware multipliers can be implemented using similar architecture, and the difference between the two bypassing multipliers lies in the input signals of the AHL. According to the bypassing selection in the columnor row-bypassing multiplier, the input signal of the AHL in the architecture with the column-bypassing multiplier is the multiplicand, whereas that of the row-bypassing multiplier is the multiplicator. Razor flip-flops can be used to detect whether timing violations occur before the next input pattern arrives.

COLUMN BYPASSING:

For a low-power column-bypassing multiplier, the addition operations in the (i+1)-th column can be bypassed if the bit, ai, in the multiplicand is 0, In the multiplier design, the modified FA is simpler than that in the row bypassing multiplier. Each modified FA in the CSA array is only attached by two tri-state buffers and one 2-to-1multiplexer. As the bit, ai, in the multiplicand is 0, their inputs in the (i+1)-th column will be disabled and the carry output in the column must be set to be 0 to produce the correct output. Hence, the protecting process can be done by adding an AND gate at the outputs of the last row of CSAs. The common multiplication method is "add and shift" algorithm. In parallel multipliers number of partial products to be added is the main parameter that determines the performance of the multiplier. To reduce the number of partial products to be added, Modified Booth algorithm is one of the most popular algorithms.



VARIABLE-LATENCY DESIGN:

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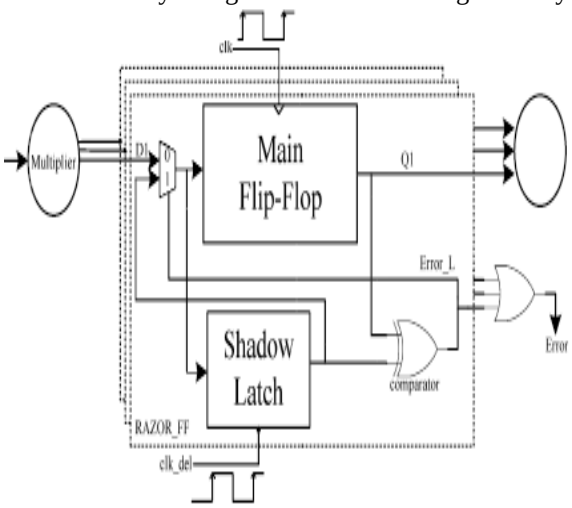
Page:7830-36

the variable-latency design was proposed to reduce the timing waste occurring in traditional circuits that use the critical path cycle as an execution cycle period. The basic concept is to execute a shorter path using a shorter cycle and longer path using two cycles. Since most paths execute in a cycle period that is much smaller than the critical path delay, the variable-latency design has smaller average latency.

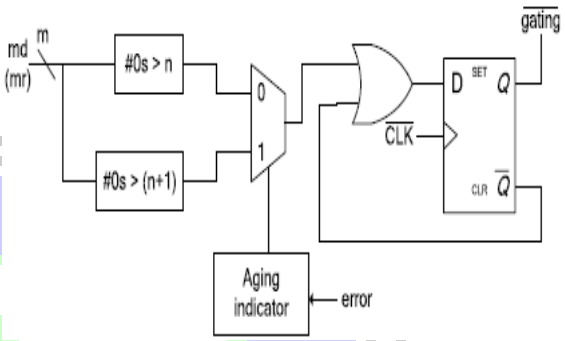


Razor flipflops

Above figure shows the details of Razor flip-flops. A 1-bit Razorflip-flop contains a main flip-flop, shadow latch, XOR gate, and mux. The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal. If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result. If errors occur, the Razor flip-flop will set the error signal to 1 to notify the system to reexecute the operation and notify the AHL circuit that an error has occurred.

AHL Circuit:

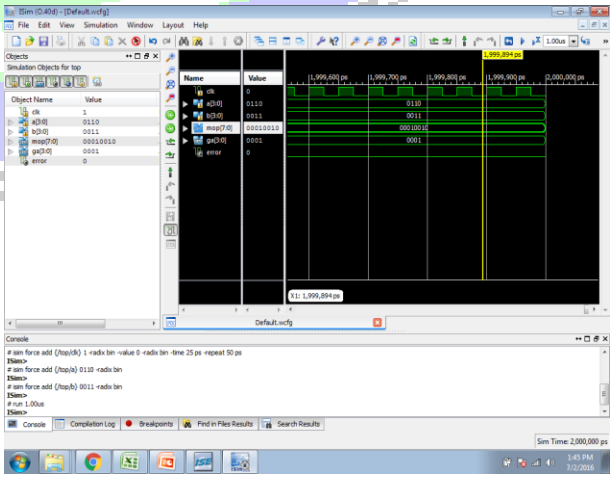
The AHL circuit contains an aging indicator, two judging blocks, one mux, and one D flip-flop. The aging indicator indicates whether the circuit has suffered significant performance degradation due to the aging effect. The aging indicator is implemented in a simple counter that counts the number of errors over a certain amount of operations and is reset to zero at the end of those operations. If the cycle period is too short, the column- or row-bypassing multiplier is not able to complete these operations successfully, causing timing violations. These timing violations will be caught by the Razor flip-flops, which generate error signals.



If errors happen frequently and exceed a predefined threshold, it means the circuit has suffered significant timing degradation due to the aging effect, and the aging indicator will output signal 1; otherwise, it will output 0 to indicate the aging effect is still not significant, and no actions are needed. The first judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand (multiplicator forthe row-bypassing multiplier) is larger than n and the second judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand is larger than n + 1.

RESULT:

SIMULATION:



CONCLUSION:

This paper proposed an aging-aware variable latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to increased delay. our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electro migration and use the worst case delay as the cycle period. The experimental results show that our proposed architecture with 8x8 multiplication using Baugh-wooley multiplication is efficiently useful in all type of applications.

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