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A SINGLE PHASE PV INVERTERS TOPOLOGY WITH A SERIES CONNECTED ENERGY BUFFER

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ABSTRACT-Module integrated converters (MICs) have been underrapid development for single-phase grid-tied photovoltaic applications.The capacitive energy storage implementation for thedouble-line-frequency power variation represents a differentiatingfactor among existing designs. This paper introduces a newtopology that places the energy storage block in a series-connectedpath with the line interface block. This design provides independentcontrol over the capacitor voltage, soft-switching for allsemiconductor devices, and the full four-quadrant operation withthe grid. The proposed approach is analyzed and experimentallydemonstrated.

Index Terms—AC module, bidirectional power transfer, cycloconverter,dc-ac power converters, distributed power generation,double line-frequency ripple, grid-connected PV systems, highfrequencyac-link, module integrated converter (MIC), multiportcircuit, photovoltaic (PV) inverter, photovoltaic power systems, resonantpower converters, single-phase energy storage, single-phaseinverters, single-stage inverters, switching circuits, zero voltageswitching
.

INTRODUCTION

GRID-TIED inverters for photovoltaic systems representa rapidly developing area. Module-integrated converters(MICs), sometimes known as microinverters, are designed tointerface a single, low-voltage (25–40 V, typically) panel to theac grid [1]–[5]. Such converters provide a number of benefits:ease of installation, system redundancy, and increased energycapture in partially shaded conditions [6].MICs typically target single-phase electrical systems (e.g.,at 240 V), and are typically restricted to the unity power factoroperation [8]. Therefore, the converter must deliver averagepower plus a time-varying power component at twice the linefrequency, while drawing a constant power from the PV module.Fig. 1 illustrates the power transfer versus time for the gridand the PV module, with the shaded area between the curves Indicating the temporal energy storage required for the inverter.To model this transfer of energy through the converter, a generalized Three-port system can be used. The constant power source

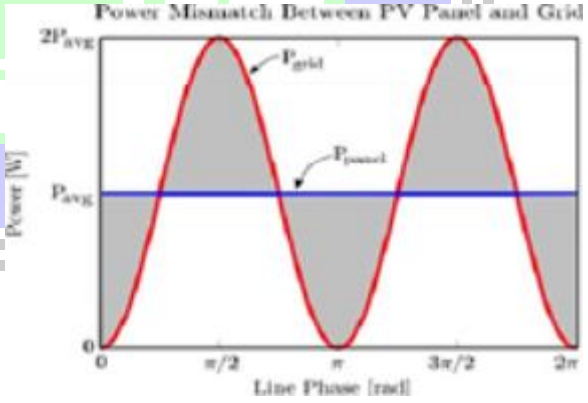


Fig. 1. Power flow mismatch between the grid and a constant power sourceresults in the shaded area, representing the required energy storage.

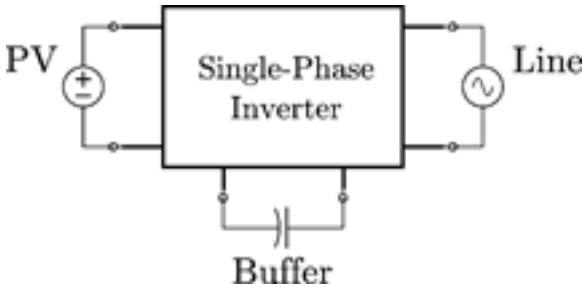


Fig. 2. Generalized grid-connected power converter, visualized as a three-portsystem.

Of the PVand the sinusoidal power load of the grid are illustratedin Fig. 2, and can be written as

$$P_{pv}=P_{avg}$$

When no reactive power is transferred. The energy storage buffermust absorb and deliver the difference in power between thesetwo ports; specificallyInverters investigated in the past (see the literature reviewscan be classified by the location and the operationof the energy storage buffer within the converter. Most singlestagetopologies, such as flyback and ac-link converters, placecapacitance in parallel with the PV panel. This is aneffective low-complexity implementation, but to avoid interfering

With the maximum peak-power tracking (MPPT) efficiency,substantial energy storage is required to limit the voltage rippleacross the panel. A second common method involves two completecascaded conversion stages, providing energy storage atan intermediate dc bus. This arrangement can be implementedwith less energy storage than the previous method, as a largervoltage fluctuation on the intermediate bus can be tolerated

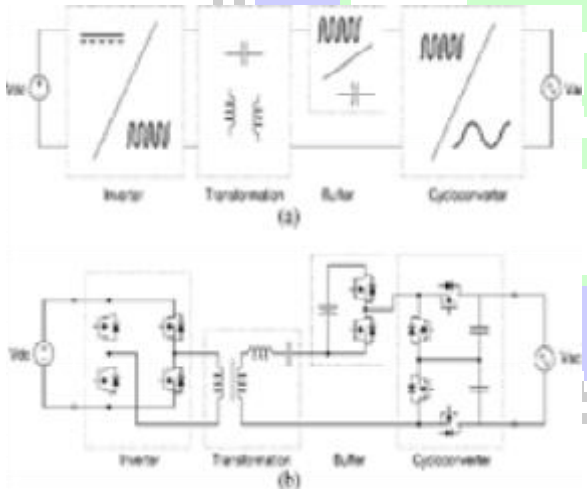


Fig. 3. Proposed photovoltaic module-integrated converter: (a) block diagramand (b) schematic

Without impacting the MPPT operation. The removal of theenergy storage from the input also improves the transient responsefor peak-power tracking, as the PV module voltage canbe controlled with a much higher bandwidth.One drawback common to both of the energy storage methodsdescribed previously involves the typical use of electrolyticcapacitors for the dc energy storage. Electrolytic capacitors aretraditionally selected due to their high energy density, but sufferfrom the stigma of long-term failure rates. As MICs are typicallymounted on the frame or backsheet of the PV moduleassembly, the high temperatures can accelerate aging processesfor many of the internal components. To address this, focus

is placed on improving converter efficiency (i.e., reduction inthermal output) and transitioning to the use of higher-reliabilitycapacitors. Recent developments in converter topologies haveincluded “third-port” systems, providing active controlof the energy storage stage, independent of the input andoutput voltages. This reduces the required energy storage, andprovides the opportunity for less energy-dense film capacitorsto be used.

The power converter presented in this paper implements a newtype of third-port topology, where the energy storage (buffer)Block is placed “in series” with the line voltage interface. Thetopology achieves high efficiencies with its continuous constantpoweroperation, zero-voltage switching (ZVS) capability for alldevices, and reduced volt-seconds applied to the high-frequencytransformer.

II. PROPOSED SOLUTION

The block diagram and schematic in Fig. 3 illustrate the fourfunctional blocks of the converter: the high-frequency resonantinverter, transformation stage, energy buffer, and cycloconverter.Each is connected electrically in series, with a common highfrequency

Resonant current linking them together.At first glance, this series-connected configuration would

Seem to impose a heavy conduction-loss penalty. However, scalingup device sizes appropriately can reduce this impact, and

The switching losses associated with large MOSFET devicescan be greatly reduced through soft-switching techniques. Additionally, the resistive channel structure allows current toflow both directions through the device, allowing for bidirectionalpower flow in each block of the converter. This is incontrast with devices such as IGBTs, SCRs, and diodes whichallow current flow in a single direction and impose a fixed on statevoltage drop. Additionally, the figure-of-merit for MOSFETshas improved steadily since their introduction, particularlywith the recent charge-compensation principles. This hasallowed high-voltage silicon MOSFETs to surpass the “silicon

Limit” and become viable for voltage ranges once relegatedto low-frequency IGBTs. Additionally, the emergence ofwide-band gap FET-based device structures, implemented in SiCand GaN, have the potential to meet these same voltage levels

While dramatically reducing the on-state resistance and undesirabledevice parasitics . This historical semiconductordevice progress, combined with these and other anticipated futuredevelopments, are a motivating factor in the elimination ofp-n junction devices in the topology. This study shows that thisapproach provides high efficiency with presently available devices,and is

anticipated to scalewith the improvements in devicetechnology. Even with the departure from traditional converterdesign, the well-known methods and algorithms forMPPT,Gridsynchronization and islanding detection can continueto be used.

To place the series-buffer topology in context, a comparativelisting of both commercial and academic work is presentedin Table I. At the expense of slightly higher complexity, theproposed converter provides a number of additional capabilitieswhile achieving an efficiency that matchespresently available designs.

III. TOPOLOGY OPERATION AND ANALYSIS

At a very high level, the converter operation is closely relatedto the ac-link family of topologies. Here, the switchingwaveforms of all three series-connected blocks are responsible for generating the intermediate high-frequency current waveform.

This can be seen in Fig. 4, where each active switchingblock is replaced with an idealized square-wave voltage source,and connected in series with the resonant circuit. To modulatepower flow through the converter, each block uses the resultingseries current as a reference, to which it readjusts its switching

Waveform appropriately.

The interdependence of the resonant current and switchingbehavior of the three blocks presents a challenge for directlyevaluating the full converter operation. To ease this, the analysisis performed with two simplifying approximations: 1) thequality factor of the series resonant circuit is sufficiently highto approximate it as a sinusoidal current source operating at theswitching frequency; and 2) the voltage at each terminal of theconverter (PV, buffer, and line) changes slowly enough, relativeto the switching frequency, that they can be approximated asconstant over a switching cycle. With these, the converter canthen be decoupled into the the two circuits in Fig. 5, separatedsuch that the dc-connected inverter and transformation blocksare grouped into the *primary* side, and the buffer and cycloconverterare grouped into the *secondary* side. This permits the two

	This Work	(1)	[16]	[22]	[23]	(2)	(3)	[9]	[10]
Topology	Series-Buffer	Flyback + Unfolder			Boost + ac-Bridge			Ac-Link	Parallel-Buffer
Energy Storage	Independent	Input			Intermediate DC			Input	Independent
Input Voltage (V)	25-40	22-36	25-50	25-45	20-40	25-37	30-50	25-40	–
Rated Power (W)	200	215	200	215	250	250	250	175	200
CEC Efficiency (%)	95.5	96	<95	<95.5	95	95	96	95.9	–
Reactive Power	Yes	No	No	No	Yes	Yes	Yes	Yes	Yes
Complexity	High	Low			Medium			Medium	High

All units are specified with a nominal 230-240V, 50-60 Hz mains interface

[1] Enphase Energy, M215-60-2LL

[2] SolarBridge Pantheon II, P250LV-240

[3] Power-One, MICRO-0.25/0.3-I-OUTD-US-208/240

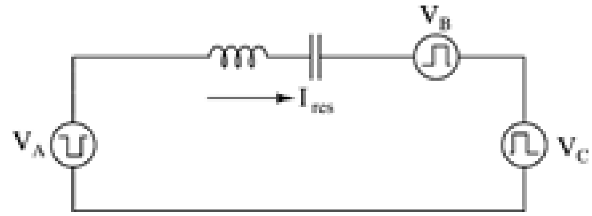


Fig. 4. Proposed topology of Fig. 3, where each active switching block isreplaced with a square-wave voltage source. The applied voltage of all threeblocks results in a high-frequency series current which links each block together.

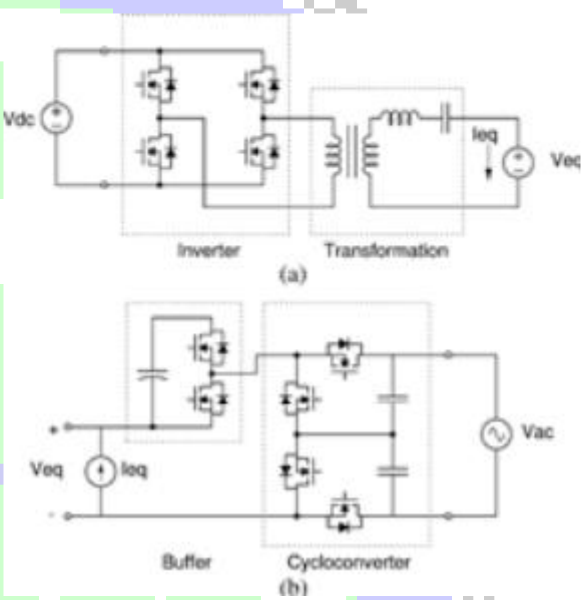


Fig. 5. Equivalent circuits representing the
(a) primary and
(b) secondarysides, decoupled by approximating the output of the transformation stage as acurrent source.

Circuits to be analyzed separately, which motivates the designprocess outlined in this section.

A. Switch Modulation

Both the primary and secondary sides of the converter areconstructed from a number of canonical totem-pole structures.The buffer is composed of one such block, where the energy storagevoltage is represented as unipolar, while the line-interfacedcycloconverter is composed of two such blocks, in a commonsourcelayout (each providing operation under opposite voltagepolarities).

The modulation of power through the simple circuit in Fig. 6 is accomplished by controlling the switching of the voltagewaveform $v(t)$ relative to the series resonant current $i(t)$.This is shown in in Fig. 7 where the resonant current

and

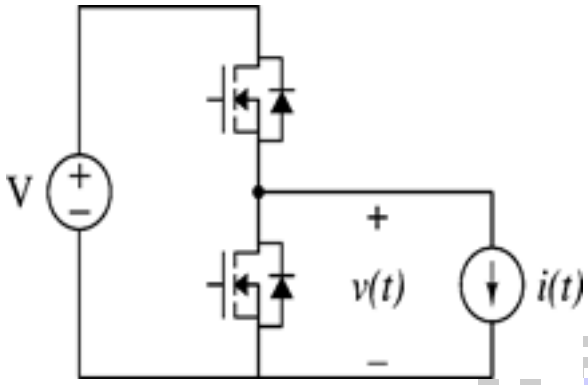
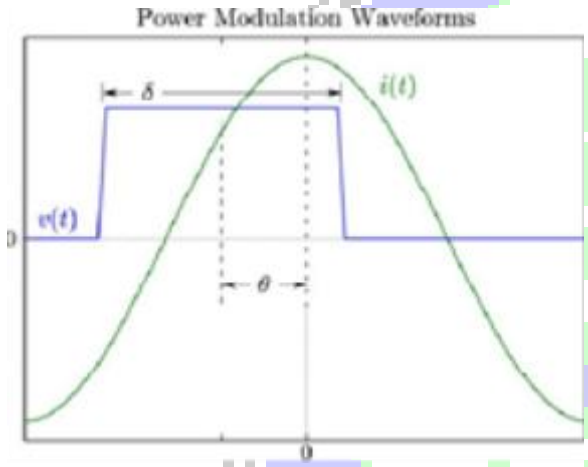


Fig. 6. Constituent sub circuit of the buffer and cycloconverter blocks from Fig. 5(b).



in Fig. 7, illustrating the control parameters δ and θ.
Switching-voltagewaveforms are illustrated with the variables $\delta$and θ, corresponding to duty-cycle and phase-shift parameters,respectively. The average power delivery over a switching cyclecan then be expressed as a function of these components through
Whereδ and θ are expressed in radians.

This same resultcan also be reached by representing the voltage and currentwaveforms as phasor quantities (at the switching frequency). Itis important to note that for a given voltage, current, and powerrequirements, a continuum of solutions exist for the controlvariables, providing the flexibility to implement additionalconstraints, such as soft-switching transitions.

B. Resonant Current Magnitude

In addition to the switching parameters, the resonant currentmagnitude in (4) remains as an additional parameter for

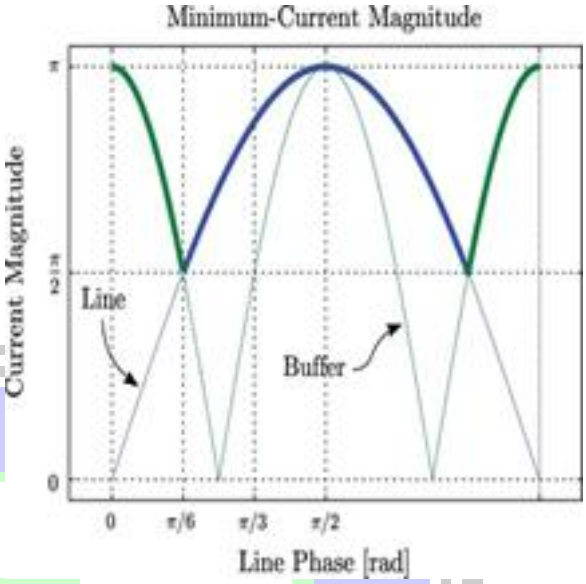


Fig. 8. Minimum resonant current magnitude requirements for the buffer blockand cycloconverter,
including the bold line indicating the envelope of currentthat meets both constraints.

C. Transformation and Inverter Design

With an understanding of the behavior of the secondary side ofthe converter, the primary-side circuit in Fig. 5(a) can be consideredwith the objective of obtaining an inverter and transformation
Combination capable of synthesizing the required resonantcurrent, as defined in the preceding section. The transformationstage is designed to provide impedance appropriate for theprimary side driving circuit; in this case it is desired to presenta positive reactance at the switching frequency for the bridge
Converter to achieve the desired ZVS conditions. Additionally,
The magnitude of the impedance must be managed such that theinverter is capable of operating over the full required voltageand power range.The varying control and behavior of the secondary half ofthe converter results in a dynamic load over a line cycle. Usingphasors, the secondary-side circuit can be approximated as acomplex impedance at the switching frequency, as shown in

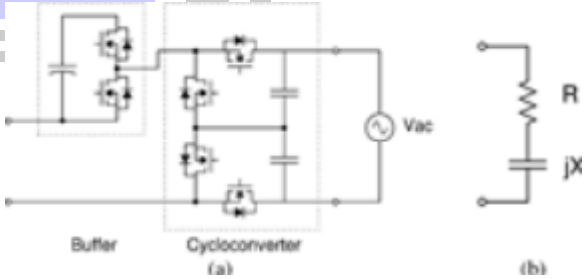


Fig. 10. (a) Buffer block and cycloconverter can be approximated as (b) thecomplex load impedance.

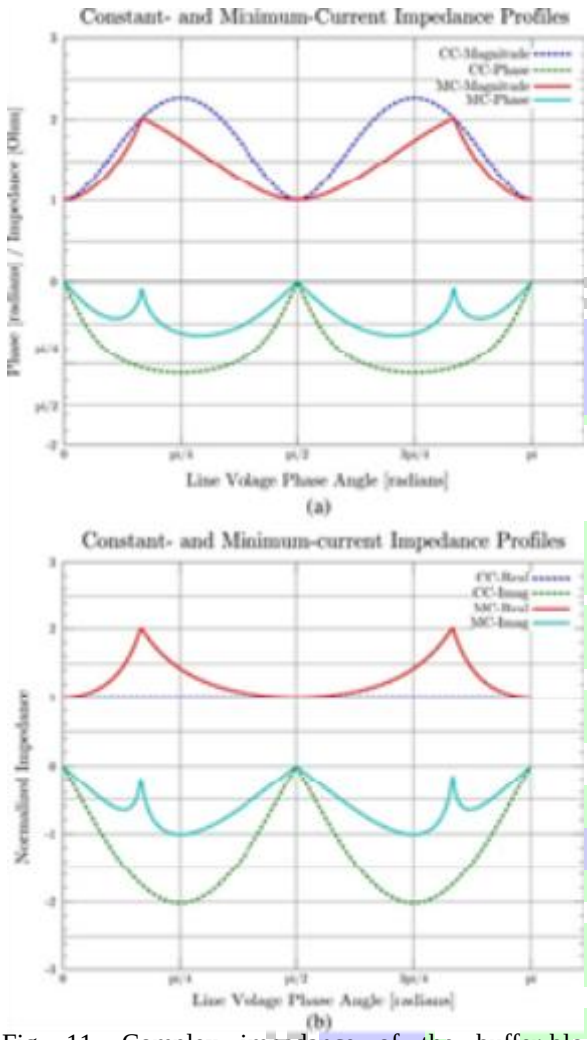


Fig. 11. Complex impedance of the buffer-block and cycloconverter are shownto vary over a line cycle based on the constant- or minimum-current drivemethod. Both the
(a) magnitude/phase and
(b) real/reactive relationships arepresented.

Fig. 10. The equivalent impedance
$Z = VC + VB/I$
of this stage is calculated and shown in Fig. 11 for both the constantand minimum-current envelopes considered previously.

Remains the same; however, its overall shape has changed.To

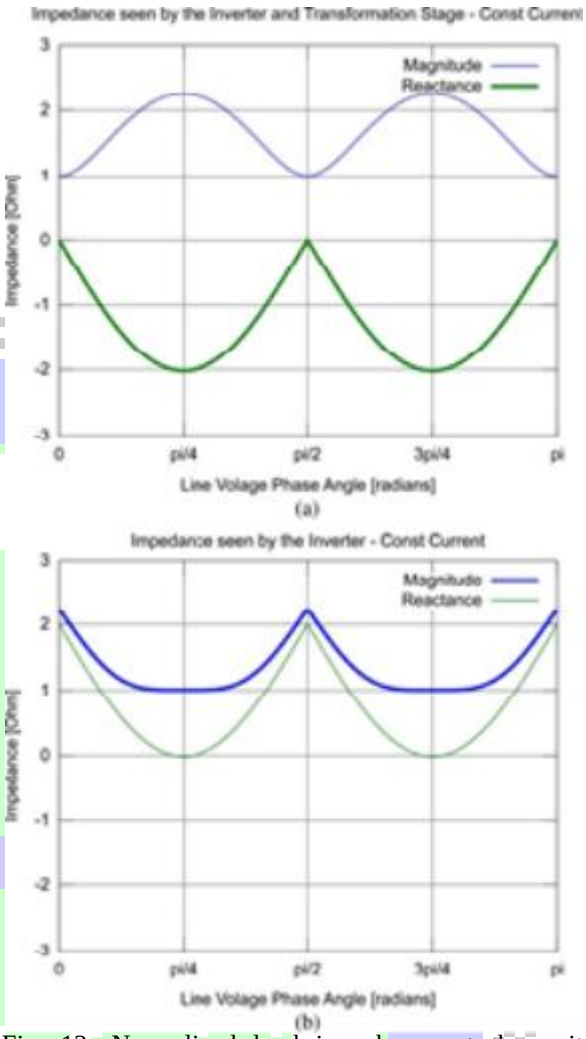


Fig. 12. Normalized load impedance, at the switching frequency, presented tothe full-bridge inverter by (a) buffer-block, and cycloconverter stages, and (b) Including the series-resonant tank.Without the inductance of the resonant tank,the reactance presented to the inverter prevents zero-voltage switching.

The lower reactive impedance for the minimum current envelopecan be understood by the length of time the blocks'phase deviate from alignment with the resonant current (0 or π).The minimum-current operation always maintains one block inphase with the current, maximizing the power factor of the resonanttank, while the constant-current method results in higherreactance.

In the transformation block, the negative reactance of the secondaryside is offset by selecting the components of the seriesresonanttank to compensate. The resulting impedance changes,

As shown Fig. 12, where the minimal required positive compensatingreactance is provided. In this case, the peak magnitude

constrained domainof the phase variables to perform a

drive this compensated load, the inverter is operated as aphase-shift full-bridge, where its applied voltage is defined inphasor form as

$V = 2V/\pi \sin(\delta/4)\, ej\theta$ (12)

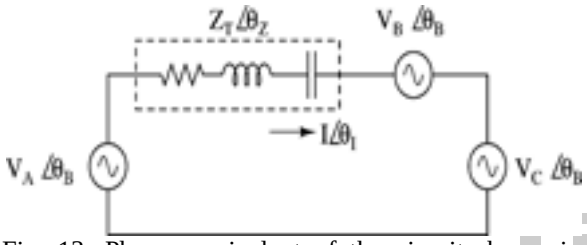


Fig. 13. Phasor equivalent of the circuit shown in Fig. 4, which approximatesthe operation of each active block as a sinusoidal voltage source.

Whereδ represents the duty cycle and θ is the phase of the voltagerelative to the resonant current waveform. With control of thisdriving voltage, and the flexibility in selecting the transformerturns ratio and the resonant tank component values, a transformationstage and inverter can be created which is capable ofsynthesizing the required resonant current.

D. Control Parameter Solutions

With the control parameters for each block defined, the interdependencebetween them can be investigated by consideringthe operation of all blocks together. To simplify the analysis, theequivalent circuit in Fig. 13 illustrates the converter in phasorform, with the voltages normalized to allow the transformationstage to be lumped into a single-series element $zT = R + jXT$,implicitly dependent on the switching frequency ($f$sw). The seriescurrent can then be defined in terms of the circuit voltagesand tank impedance, such that

$I = 1/ZT\, ej\theta Z(VAej\theta A + VB\, ej\theta B + VC\, ej\theta C)$

and the power delivery for a given voltage source k is expressedas

$Pk = 1/2Re$

For a single block, this power transfer equation requires sevenparameters: the switching frequency, and the magnitude andphase for the three voltage sources. This list can be reduced bychoosing to define one phase as the reference, eliminating it as an

Unknown. Additionally, having implemented phase-shift modulationfor the buffer and cycloconverter, in combination with

Their measurable terminal voltages, results in known voltagemagnitudes for VB and VC . This leaves the switching frequency$f$sw , phases θB , and θC , and the effective driving voltage ofthe full-bridge VA. The single-phase power flow requirementsfor the converter, given in (1)–(3), provide two independent Constraints and the remaining two are imposed by selectingan appropriate value for the switching frequency $f$sw and full bridgepulse-width δA (for control of VA). To solve for θB andθC, one can take advantage of the inherently direct search. Implementingan iterative solver is also effective, but often complicated by theexistence of multiple solutions.With a solution method in place for finding the unknownphase angles, it is repeated for additional combinations of the

A. Simulation Results

The operation and performance of the converter is measuredin two different configurations. First, the converter is operatedin dc–dc mode, stepped over a set of discrete operating pointsapproximating an ac output. Second, the converter is operatedin stand-alone dc–ac mode. In both configurations the converteris fedwith constant-voltage at its input, and pre-populatedlookup tables are used by the converter for the hardware controlparameters.The oscilloscope waveform captures in Fig. 15 are used toillustrate the switching-level operation of the converter at three

Points in the line cycle, with an output power of 100W, aninput voltage of 32 V, and a buffer voltage of 170 V. Startingat the zero crossing of the line, a line phase of 0◦ (0 V),Fig. 15(a) shows the buffer-block absorbing power, with itsswitching waveform nearly in-phase with the negative portionof the resonant current. The second capture occurs at a line phaseof 30◦ (170 V), where the buffer block and cycloconverter areeach absorbing 50W from the source, with voltage waveformsswitching complimentary to each other. At a line phase of 90◦

(340 V), shown in Fig. 15(c), the buffer and source are each providing100W to the cycloconverter, which is providing 200Wout.

In the dc–dc operation, the converter's efficiency over a linecycle was measured for five average-power levels, at an inputvoltage of 32 V.

These results, shown in Fig. 16, demonstrateefficiencies above 91% for all conditions, with peaks above98%.

These are power stage efficiencies, and the inclusion ofthe gate drive and auxiliary power accounts for an additionalloss of 1–1.8%.

This was also performed at two additional inputvoltages , resulting in an approximate CEC efficiency of 95.5%.

The converter was also operated in the full dc–ac mode, intoa 60Hz 240Vac line simulator, with an input voltage and power

Fig. 16.Simulation obtained dc input and (unfiltered) ac

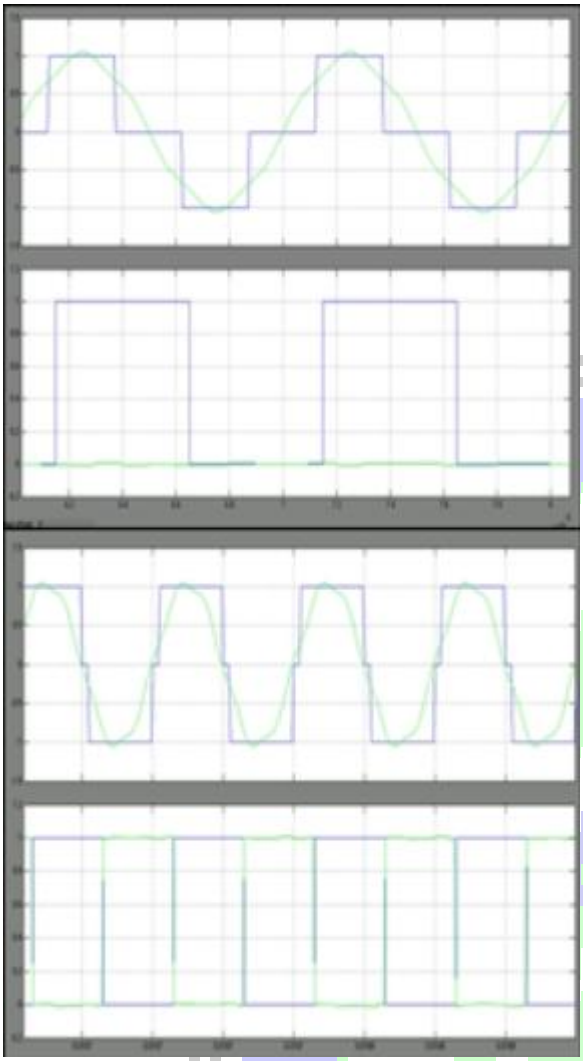
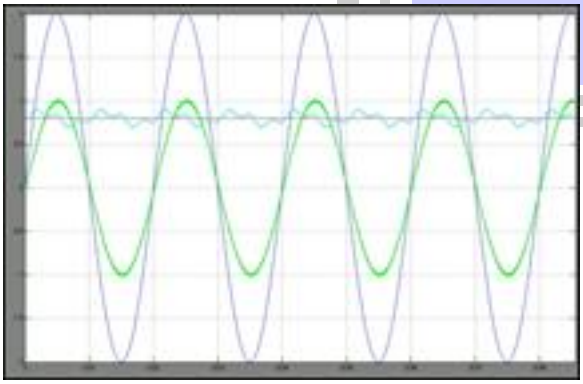


Fig. 15. Converter operation with 32V input, 100W average power, at threepoints in the line cycle: (a) 0◦, 0V; (b) 30◦, 170 V; (c) 90◦, 340 V. Waveformchannel number and color key; (1) blue: current, (2) red: full-bridge, (3) green:buffer-block, and (4) purple: cycloconverter. Channels 1 and 2 are referenced tothe top marker, while channels 3 and 4 are referenced to the bottom marker.



output waveforms,at an input voltage of 32V.Waveform channel number and color key; (1)
Blue: input current, (2) red: output current, (3) green: input voltage, (4) purple:output voltage. Channels 2 and 4 are referenced to the center marker, while
channels 1 and 3 are referenced to the bottom maker.
a control parameter lookup-table, indexed by its output voltagemeasurement.
This dc–ac operation results in a 95.3% efficiency, includingall gate and auxiliary power. The voltage and current waveformmeasurements for the dc input and ac output of the converter areshown in Fig. 17. The ideal waveforms would have a constantinput voltage and input current with a sinusoidal output currentin-phase with the output voltage; however, the measuredresults deviate slightly from this. The largest contributor to thediscrepancy comes from the uncompensated delay associatedwith voltage measurement, and more significantly, the time durationrequired to update the converter operating parameters;
a total delay of 1ms. This update latency primarily manifestsitself as an unintended phase-shift in the output current relativeto the line voltage (reactive power transfer), ultimately reflectingback as input-power ripple (seen as current ripple). Thisunintended operation also illustrates the well-behaved natureof the cycloconverter near the line zero crossings, where theopposing half-bridge circuits can be operated synchronously toprevent short-circuit conditions when the voltage polarity maybe uncertain [9].The residual current ripple drawn by the converter, intentionalor not, must be suppressed to maintain a fixed point on the PVmodule *I–V* curve. This can be achieved with a relatively smalladditional capacitance at the input, stabilizing the voltage for
MPPT. It is expected that effective compensation of the controlloop delay will reduce, if not negate, the input ripple and thisextra energy storage.

V. CONCLUSION

The converter design and implementation presented in thispaper has demonstrated a new topology with an energy-storagebuffer in the series-connected path with the line interface. Ithas an increased complexity relative to traditional designs, butallows control over the energy storage voltage and ripple, permittingthe use of electrolytic or film capacitors. It alsomaintains
the capability of reactive power transfer and high efficiency, asdemonstrated.
The presented bench prototype provides verification of thefunctionality and performance of the design process. While notthe primary focus, the standalone

dc–ac test demonstrated 95.3%efficiency under representative operating conditions (100W,32V input, 240V output), all inclusive. Further improvementson these successful results are expected with optimized magneticand online tuning of control parameters.

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