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A NEW THREE PHASE MULTILEVEL INVERTER WITH REDUCED NUMBER OF POWER ELECTRONIC COMPONENTS

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ABSTRACT- In this paper, a new configuration of a three-phase nine-level multilevel voltage-source inverter is introduced along with fuzzy logic. A multilevel dc link using fixed dc voltage supply and cascaded half-bridge is connected in such a way that the proposed inverter outputs the required output voltage levels. Here we are using fuzzy logic controller instead of using other controllers. The fundamental frequency staircase modulation technique is easily used to generate the appropriate switching gate signals. For the purpose of increasing the number of voltage levels with fewer number of power electronic components, the structure of the proposed inverter is extended and different methods to determine the magnitudes of utilized dc voltage supplies are suggested. Moreover, the prototype of the suggested configuration is manufactured as the obtained simulation and hardware results ensured the feasibility of the configuration and the compatibility of the modulation technique is accurately noted.

Index terms – Bidirectional switch, fundamental frequency staircase modulation, multilevel inverter, Fuzzy logic.

I. INTRODUCTION

On the other hand, for the purpose of improving the performance of the conventional single- and three-phase inverters, different topologies employing different types of bidirectional switches have been suggested. Comparing to the unidirectional one, bidirectional switch is able to conduct the current and withstanding the voltage in both directions. Bidirectional switches with an appropriate control technique can improve the performance of multilevel inverters in terms of reducing the number of semiconductor components, minimizing the withstanding voltage and achieving the desired output voltage with higher levels. Based on this technical background, this paper suggests a novel topology for a three phase nine-level multilevel inverter.

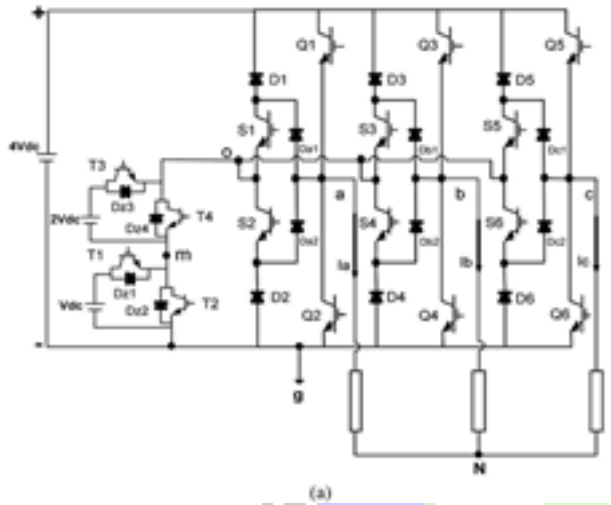
Multilevel inverters consist of a group of switching devices and dc voltage supplies, the output of which produces voltages with stepped waveforms. Multilevel technology has started with the three-level converter followed by numerous multilevel converter topologies. Different topologies and wide variety of control methods have been developed in the recent literature. The most common multilevel inverter configurations are neutral point clamped (NPC), the flying capacitor (FC), and the cascaded H-bridge (CHB). The deviating voltage of neutral-point voltage in NPC, the unbalanced voltage in the dc link of FC, and the large number of separated dc supplies in CHB are considered the main drawbacks of these topologies. Apart from these three main topologies, other topologies are introduced. Recently, asymmetrical and hybrid multistage topologies are becoming one of the most interested research area. In the asymmetrical configurations, the magnitudes of dc voltage supplies are unequal. These topologies reduce the cost and size of the inverter and improve the reliability since minimum number of power electronic components, capacitors, and dc supplies are used. The hybrid multistage converters consist of different multilevel configurations with unequal dc voltage supplies. With such converters, different modulation strategies and power electronic components technologies are needed.

The number of switching devices, insulated-gate driver circuits, and installation area and cost are significantly reduced. The magnitudes of the utilized dc voltage supplies have been selected in a way that brings the high number of voltage level with an effective application of a fundamental frequency staircase modulation technique. Extended structure for *N*-level is also presented and compared with the conventional well-known multilevel inverters. Simulation and hardware results are given and explained.

II. PROPOSED TOPOLOGY

Fig.1shows the typical configuration of the proposed three-phase nine-level multilevel inverter. Three bidirectional switches (S1–S6, Da1–Dc2), two switches–two diodes type, are added to the conventional three-phase two-level bridge (Q1–Q6). The function of these bidirectional switches is to block the higher voltage and ease current flow to and from the midpoint (o). A multilevel dc link built by a single dc voltage supply with fixed magnitude of 4*V*dc and CHB having four dc

voltage supplies of *V*dc, *V*dc and 2*V*dc, 2*V*dcare connected to (+, –, o)bridge terminals.



(a)

Fig. 1. Circuit diagram of the proposed three-phase 9-level multilevel inverter

Based on the desired number of output voltage levels, a number of CHB cells are used. Since the proposed inverter is designed to achieve nine voltage levels, the power circuit of the CHB makes use of four series cells having two unequal dc voltage supplies. In each cell, the two switches are turned ON and OFF under inverted conditions to output different voltage levels.

The first cell dc voltage supply *V*dc is added if switch T1 is turned ON leading to *V*mg= +*V*dc where *V*mg is the voltage at node (*m*) with respect to inverter ground(*g*) or bypassed if switch T2 is turned ON leading to *V*mg=0. Likewise, the second cell dc voltage supply 2*V*dc is added when switch T3 is turned ON resulting in *V*om=+2*V*dc where *V*om is the voltage at midpoint (*o*) with respect to node (*m*) or bypassed when switch T4 is turned ON resulting in *V*om= 0.The peak voltage rating of the switches of the conventional two level bridge (Q1–Q6) is 4*V*dc whereas the bidirectional switches(S1–S6) have a peak voltage rating of 3*V*dc. In CHB cells, the peak voltage rating of second cell switches (T3 and T4) is 2*V*dcwhile the peak voltage rating of T1 and T2 in the first cell is *V*dc .By considering phase *a*, the operating status of the switches and the inverter line-to-ground voltage *V*ag are given in Table I.

TABLE I:

Switching State *Sa* and Inverter Line-to-Ground Voltage

								*V*ag
	Q1	**S1**	**S2**	**Q2**	**T1**	**T2**	**T3**	**T4**	
4	on	off	off	off	on	off	on	off	+4
3	off	on	on	off	on	off	on	off	+3
2	off	on	on	off	off	on	on	off	+
1	off	on	on	off	on	off	off	on	+
0	off	off	off	On	on	off	off	on	0

It is easier to define the inverter line-to-ground voltages *V*ag, *V*bg, and *V*cg in terms of switching states *Sa*, *Sb*, and *Sc*as

$$= - \quad * \qquad (1)$$

Where $N = 5$ is the maximum number of voltage levels. The balanced load voltages can be achieved if the proposed inverter operates on the switching states depicted in Table II. The inverter may have 24 different modes within a cycle of the output waveform. According to Table II, it can be noticed that the bidirectional switches operate in 18 modes. For each mode, there is no more than one bidirectional switch in on state.

As a result, the load current commutates over one switch and one diode (for instance: in (410), the load current *I*b can flow in S3 and Db1 or S4 and Db2). Since some insulated ate bipolar transistors (IGBTs) share the same switching gate signals, the proposed configuration significantly contributed in reducing the utilized gate driver circuits and system complexity. The inverter line-to-line voltage waveforms *V*ab, *V*bc, and *V*ca with corresponding switching gate signals are depicted in Fig. 2where *V*ab, *V*bc, and *V*ca are related to *V*ag, *V*bg, and *V*cg by

$$= \begin{matrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{matrix} * \qquad (2)$$

The inverter line-to-neutral voltages *V*aN, *V*bN, and *V*cN maybe expressed as

$$= \begin{matrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{matrix} * \qquad (3)$$

It is useful to recognize that the inverter voltages at terminals *a*, *b*, and *c* with respect to the midpoint (*o*) are given by

$$= \quad - \qquad (4)$$

Where *V*og is the voltage at midpoint (*o*) with respect to ground(*g*). *V*og routinely fluctuates among three different voltage values *V*dc, 2*V*dc, and 3*V*dc as follows: +8*V*dc/3, +7*V*dc/3, +6*V*dc/3, +5*V*dc/3, +4*V*dc/3, +2*V*dc/3, 0, –2*V*dc/3, −4*V*dc/3, –5*V*dc/3, –6*V*dc/3, −7*V*dc/3, and –8*V*dc/3.

It is worth noting that all simulated waveforms are obtained at $t1=t2 = \cdots = t24 = 0.02/24$ s.

$$= 2 \begin{cases} + \quad + \quad \le 5 \\ + \quad + \quad = 6 \\ + \quad + \quad \ge 7 \end{cases} \qquad (5)$$

The simulated voltage waveforms of *V*ag, *V*og ,*V*ao and *V*aN based on (1)–(5) are shown in Fig. 3 where, for instance, 13sequent voltage steps are seen in *V*aN waveform as follows:

TABLE II
SWITCHING STATES SEQUENCE OF THE PROPOSED INVERTER WITHIN ONE CYCLE

	Period T[s]	ON switches Leg a	ON switches Leg b	ON switches Leg c	ON switches Cascaded half-bridge			
400	t1	Q1	Q4	Q6	T1, T4	4	0	0
410	t2	Q1	S3, S4	Q6	T1, T4	4		0
420	t3	Q1	S3, S4	Q6	T2, T3	4	2	0
430	t4	Q1	S3, S4	Q6	T1, T3	4	3	0
440	t5	Q1	Q3	Q6	T1, T3	4	4	0
340	t6	S1,S2	Q3	Q6	T1, T3	3	4	0
240	t7	S1,S2	Q3	Q6	T2, T3	2	4	0
140	t8	S1,S2	Q3	Q6	T1, T4		4	0
040	t9	Q2	Q3	Q6	T1, T4	0	4	0
041	t10	Q2	Q3	S5, S6	T1, T4	0	4	0
042	t11	Q2	Q3	S5, S6	T2, T3	0	4	
043	t12	Q2	Q3	S5, S6	T1, T3	0	4	2
044	t13	Q2	Q3	Q5	T1, T3	0	4	3
034	t14	Q2	S3, S4	Q5	T1, T3	0	3	4
024	t15	Q2	S3, S4	Q5	T2, T3	0	2	4
014	t16	Q2	S3, S4	Q5	T1, T4	0		4
004	t17	Q2	Q4	Q5	T1, T4	0	0	4
104	t18	S1,S2	Q4	Q5	T1, T4		0	4
204	t19	S1,S2	Q4	Q5	T2, T3	2	0	4
304	t20	S1,S2	Q4	Q5	T1, T3	3	0	4
404	t21	Q1	Q4	Q5	T1, T3	4	0	4
403	t22	Q1	Q4	S5, S6	T1, T3	4	0	3
402	t23	Q1	Q4	S5, S6	T2, T3	4	0	2
401	t24	Q1	Q4	S5, S6	T1, T4	4	0	

In order to plot the space vector diagram of the proposed inverter in a stationary *d*–*q* reference frame, the following equations can be used to derive *d* and *q* voltage components for all inverter vectors:

$$= \frac{}{(\ )}(2 \quad - \quad - \quad) \qquad (6)$$

$$= \frac{}{\sqrt{(\ )}}(\quad - \quad)\ (7)$$

$$V = \quad - \qquad (8)$$

For all switching states presented in Table II, Fig. 4 shows the space vector diagram for the proposed topology.

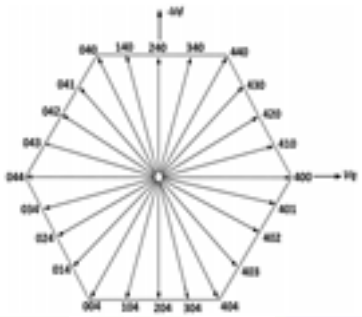


Fig.2.Switching states vectors of the proposed inverter in *d*–*q* reference frame.

SWITCHING ALGORITHM

The staircase modulation can be simply implemented for the proposed inverter. Staircase modulation with selective harmonics the most common modulation technique used to control the fundamental output voltage as well as to eliminate the undesirable harmonic components from the output waveforms. An iterative method such as the Newton–Raphson method is normally used to find the solutions to (*N*–1) nonlinear transcendental equations. The difficult calculations and the need of high performance controller for the real application are the main disadvantages of such method.

$$= \frac{*}{} * \begin{matrix} \cos(\quad) \\ \cos(\quad - \quad) \\ \cos(\quad + \quad) \end{matrix} + \quad - \quad * \begin{matrix} 1 \\ 1 \\ 1 \end{matrix} \qquad (9)$$

Where *wt* is the electrical angle. Or

$$= \frac{*}{} * \begin{matrix} \cos(\quad) \\ \cos(\quad - \quad) \\ \cos(\quad + \quad) \end{matrix} + \quad - \quad * \begin{matrix} 1 \\ 1 \\ 1 \end{matrix}$$

$$1 - \quad \cos(3 \quad) * \qquad (10)$$

fundamental voltage without causing over modulation. As a result, M_a can reach to 1.15 and *Sa*, *Sb*, and *Sc* can be simply determined by integrating the reference line-to-ground voltages as

$$= \quad _ \quad * \quad - \quad - \qquad (11)$$

Comparison of the proposed modulation method with the staircase modulation with the selective harmonic method shows that the proposed modulation features less time and needs simple calculations. The inverter's operating switching states *Sa*, *Sb*, and *Sc*and corresponding switching gate signals based on the proposed modulation method are shown in Fig. 5.It is clear that

TABLE III
SWITCHING STATE Sa1 AND INVERTER LINE-TO-GROUND VOLTAGE V_{ag} AT M_a <0.9 (LEG *a*)

Sa1	Q1	S1	S2	Q2	T1	T2	T3	T4	
2	On	Off	Off	Off	Off	On	On	Off	+4Vdc
1	Off	On	On	Off	Off	On	On	Off	+2Vdc
0	off	off	off	on	Off	On	On	Off	0

that the switching gate signals are generated within 24 different modes starting from (044) to (034).Since the proposed inverter has been designed to achieve nine voltage levels, the modulation index must be within range0.9 ≤ M_a ≤ 1.15. For modulation index M_a <0.9, only two dc voltage supplies $4V_{dc}$ and $2V_{dc}$ are utilized and the behaviour of the proposed inverter becomes similar to the three-level multilevel inverter. Using (9)–(11) and substituting N = 3, the inverter's operating switching states *Sa*, *Sb*, and *Sc*at M_a <0.9 can be defined. The operation principle of the proposed inverter at M_a <0.9 is illustrated in Table III. Fig. 6(a) and (b) shows the inverter line-to-line voltage waveforms at nine different modulation indices including the over modulation operation M_a = 0.8,0.9, 1.05, 1.15, and 1.3.

IV. EXTENDED STRUCTURE

It is noticeable that there is possibility to reach an output voltage with higher number of steps in the proposed multilevel inverter by extending the CHB circuit. Such extending can be done by adding more half-bridge cells connected in series as shown in Fig. 7(a) and (b). In order to achieve the desired number of voltage levels, three methods can be followed to determine the magnitudes of utilized dc voltage supplies.

1) All cells have an equal dc supply in magnitude.

$$= (\quad 1) \quad = (1 + \quad) \qquad (13)$$

Where *n* is the number of utilized cells. The maximum number of voltage steps is related to the number of utilized cells by

$$N = n + 2 \qquad (14)$$

The number of operation modes that makes the switching states sequence achieves the required output voltage waveform

$$M=6(N-1) \qquad (15)$$

2) The magnitude of dc voltage supply used in each and every cell in a particular inverter is obtained as follows:

$$= \qquad (16)$$

$$= 2 \qquad (17)$$

$$= \qquad (18)$$

$$= (\quad - 1) \quad = \quad 1 + \frac{(\quad)}{} \qquad (19)$$

$$N = 2 + \frac{(\quad)}{} \qquad (20)$$

$$M = 6(N-1) \qquad (21)$$

3) By making a binary (power of 2) relationship between thedc supplies of the CHB structure as follows:

$$= 2^{(\quad)}(\quad) \qquad (22)$$

$$= 2^{(\quad)}(\quad) \qquad (23)$$

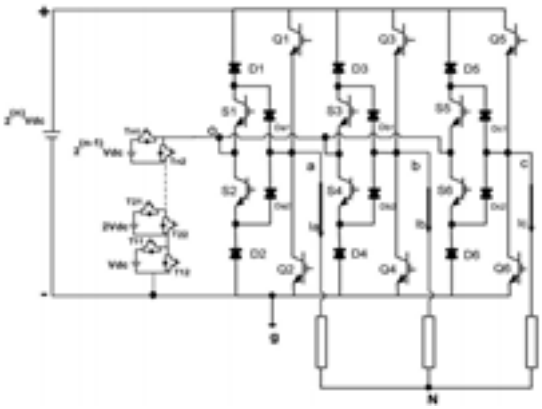


Fig.3. Circuit diagram of the proposed three-phase N-level multilevel inverter

$$= 2^{(\quad)}(\quad) \qquad (24)$$

$$= (\quad - 1) \quad = \quad 1 + \quad 2 \quad = (2 \quad) \qquad (25)$$

$$N=1+2 \qquad (26)$$

M=6(N 1) (27)

Table IV illustrates some characteristics of the proposed methods.

TABLE IV
COMPARISON OF THE MAXIMUM NUMBER OF VOLTAGE LEVELS WITH THE REQUIRED VALUE OF DC VOLTAGE SUPPLIES AMONG THE PROPOSED METHODS

Number of cells	1st Method		2nd Method		3rd Method	
n	N	M	N	M	N	M
2	4	18	3	5	24	4	5	24	4
3	5	24	4	8	42	7	9	48	8
4	6	30	5	12	66	11	17	96	16
5	7	36	6	17	96	16	33	192	32
6	8	42	7	23	132	22	65	384	64

Based on the comparison carried among the proposed methods, the following are some observations.
1) Comparing to the second and third methods, the first method has a high modularity degree since the symmetric structure of CHB makes use of equal dc voltage supplies. This method helps the proposed inverter to reach all maximum number of voltage levels (4, 5, 6, 7, 8,...,*N*).

2) Since the second and third methods use the asymmetrical structure of CHB, the proposed inverter can reach the required output voltage and the maximum number of voltage levels such as 5, 8, 9, 12, 17,...with less number of dc voltage supplies and power electronic components.

COMPARISON STUDY

In order to investigate the capability of the suggested configuration, the proposed inverter is compared with different types of multilevel inverters such as NPC, FC, and CHB. It is evident that the suggested three-phase *N*-level multilevel inverter can considerably minimize the required number of power components. For the same number of output voltage levels ($N \geq 4$),Table V explains the required number of dc voltage supplies, switches, clamping diodes, control signals, and balancing capacitors of the proposed *N*-level inverter compared with three existing inverters NPC, FC, and CHB. As shown in Fig. 8,it can be noticed that nearly more than two-thirds of number of switches can be counted out as *N* increases. For instance, at the same number of voltage levels $N = 17$, and compared with the existing multilevel inverters which require 96 switches, the required number of switches for the proposed inverter is less since it requires 42 switches based on the first method, 22switches based on the second method, and 20 switches based on the third method. On the other hand, it is well known that the voltage and current ratings of the power components have an effect on the cost and realization of the multilevel inverter. Assuming that all power components have an equal current rating which is the rated current of the load (*IL*), the voltage ratings of these components depend on the magnitude of dc voltage supplies, voltage stress, and structure of the inverter. Considering that all inverters have the same input dc link which equals$(N–1)V_{dc}$, Table VI illustrates the rating requirements for the proposed inverter comparing with the rating requirements fort he existing inverters. It is observed that the inverter employs switching devices with high voltage rating. That results in high cost per-switch. Since the topology is introduced with reduced number of switches, gate driver circuit, diodes and no clamping capacitors are involved, the semiconductor devices expenses are considerably recovered.

III. POWER CONVERSION EFFICIENCY AND TOTAL HARMONICDISTORTION (THD%)

In order to determine the efficiency of the proposed inverter, it is necessary to determine the value of conduction and switching power losses generated by the semiconductor components. Basically, the main losses in semiconductor components such as IGBTs and diodes are categorized into two groups: conduction loss (P_{con}) and switching loss (P_{sw}) as follows:

$$= \int ( ) + \int ( ) ( ) \quad (28)$$

$$= \int ( ) \quad (29)$$

Where $E_{on}(t)$ is a turn-on loss and $E_{off}(t)$ is a turn-off loss. Switching losses $E_{on}(t)$ and $E_{off}(t)$ are experienced during the ON and OFF states, respectively. While $E_{rr}(t)$ is the reverse recovery loss of the diode, the majority of switching loss, which is experienced when the diode is turned OFF (OFF state)

$$= \int_0 ( ) \quad (30)$$

$$= \int_0 ( ) \quad (31)$$

Conduction power losses of IGBT and diode are approximated based on their forward voltage drops $V_{on\ IGBT}$,$V_{on\ diode}$, and the instantaneous current $i(t)$ flowing

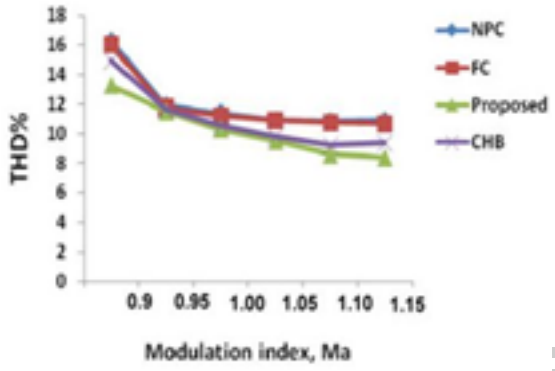


Fig. 5. NPC, FC, CHB, and proposed inverter: line-to-line voltage THD%versus *Ma* .

Moreover, the proposed inverter has been tested under different modulation indices (M_a = 0.9, 1, and 1.15). THD% of theoutput voltage can be calculated by

$$THD\% = \frac{\sqrt{\sum^{\infty}}}{} \times 100\% \quad (41)$$

where V_1 and V_k are the fundamental component and harmonic order, respectively. NPC, FC, and CHB multilevel inverters have been tested under the same operating conditions. The goal of this test is to compare the proposed inverter with the existing inverters in term of THD%. Fig. 10 depicts THD% of the line to line voltage for all inverters within specific range of modulation indices [0.9–1.15]. It can be seen that the THD% of all inverter is slightly different. The measured values of THD% for the proposed inverter are within a range of 8.4–13.25%. As a result, the proposed inverter essentially adds the attractive aspects of the traditional two-level inverter such as less power components, simple working principle, and minimum conduction power loss to the main advantages of the multilevel inverter such as low THD% and high output voltage quality.

IV. FUZZY LOGIC CONTROLLER

In FLC, basic control action is determined by a set of linguistic rules. These rules are determined by the system. Since the numerical variables are converted into linguistic variables, mathematical modeling of the system is not required in FC. The FLC comprises of three parts: fuzzification, interference engine and defuzzification. The FC is characterized as i. seven fuzzy sets for each input and output. ii. Triangular membership functions for simplicity. iii. Fuzzification using continuous universe of discourse. iv. Implication using Mamdani's, 'min' operator. v. Defuzzification using the height method.

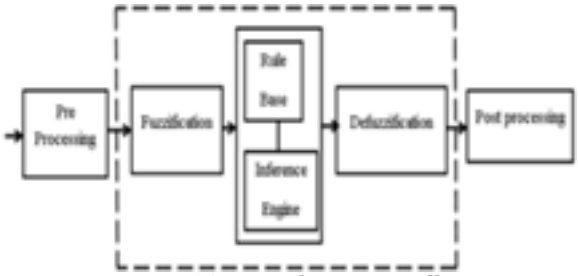


Fig.(6) Fuzzy logic controller

Fuzzification: Membership function values are assigned to the linguistic variables, using seven fuzzy subsets: NB (Negative Big), NM (Negative Medium), NS (Negative Small), ZE (Zero), PS (Positive Small), PM (Positive Medium), and PB (Positive Big). The partition of fuzzy subsets and the shape of membership CE(k) E(k) function adapt the shape up to appropriate system. The value of input error and change in error are normalized by an input scaling factor

Table I Fuzzy Rules

Change in error	Error NB	NM	NS	Z	PS	PM	PB
NB	PB	PB	PB	PM	PM	PS	Z
NM	PB	PB	PM	PM	PS	Z	Z
NS	PB	PM	PS	PS	Z	NM	NB
Z	PB	PM	PS	Z	NS	NM	NB
PS	PM	PS	Z	NS	NM	NB	NB
PM	PS	Z	NS	NM	NM	NB	NB
PB	Z	NS	NM	NM	NB	NB	NB

In this system the input scaling factor has been designed such that input values are between -1 and +1. The triangular shape of the membership function of this arrangement presumes that for any particular E(k) input there is only one dominant fuzzy subset. The input error for the FLC is given as

$$E(k) = \frac{(\quad)\qquad(\quad)}{(\quad)\qquad(\quad)} \quad (14)$$

$$CE(k) = E(k) - E(k\text{-}1) \quad (15)$$

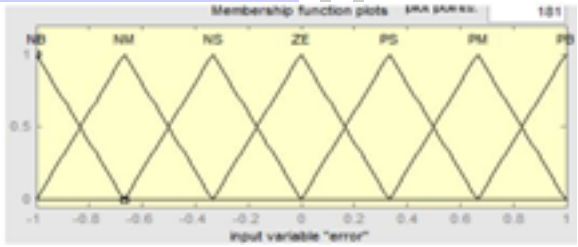


Fig.(7) Membership functions

Inference Method: Several composition methods such as Max–Min and Max-Dot have been proposed in the literature. In this paper Min method is used. The output membership function of each rule is given by the

minimum operator and maximum operator. Table 1 shows rule base of the FLC.

Defuzzification: As a plant usually requires a non-fuzzy value of control, a defuzzification stage is needed. To compute the output of the FLC, „height" method is used and the FLC output modifies the control output. Further, the output of FLC controls the switch in the inverter. In UPQC, the active power, reactive power, terminal voltage of the line and capacitor voltage are required to be maintained. In order to control these parameters, they are sensed and compared with the reference values. To achieve this, the membership functions of FC are: error, change in error and output.

The set of FC rules are derived from

$$u=-[\alpha E + (1-\alpha)*C]$$

Where α is self-adjustable factor which can regulate the whole operation. E is the error of the system, C is the change in error and u is the control variable. A large value of error E indicates that given system is not in the balanced state. If the system is unbalanced, the controller should enlarge its control variables to balance the system as early as possible. set of FC rules is made using Fig.(7) is given in Table 1.

V. MATLAB CIRCUIT MODEL

MATLAB/Simulink model of the proposed inverter shown in Fig. 1 has been developed to study the conduction and switching power losses. The proposed inverter is designed to deliver output power of P_{out} = 1.9 kW. To simplify the losses calculation, a curve-fitting tool of MATLAB is used to approximate these curves by exponential equations [35].

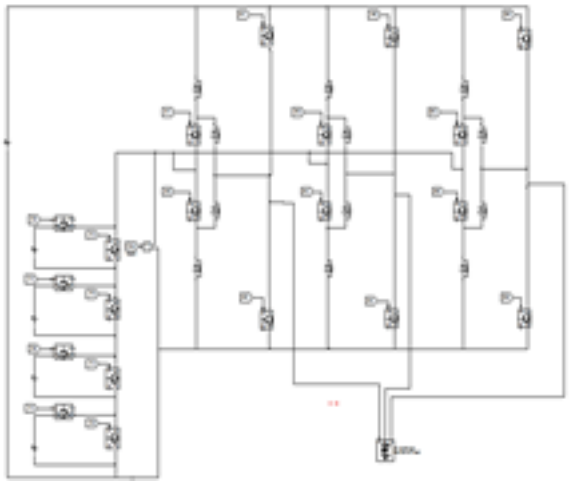


Fig.8. MATLAB Circuit diagram of the proposed three-phase 9-level multilevel inverter

VI. SIMULATION RESULTS

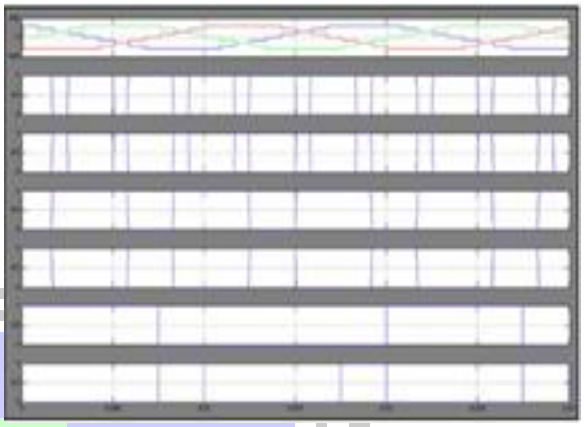


Fig.9. Simulated waveforms of *V*ab, *V*bc, and *V*ca with corresponding switching gate signals for the proposed inverter at fundamental frequency *f* = 50 Hz.

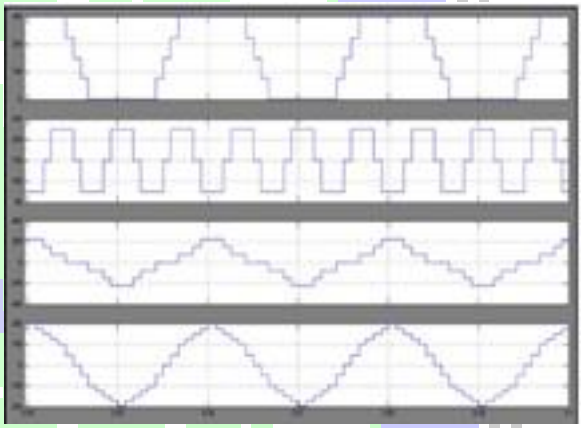


Fig. 10. Simulated waveforms of *V*ag, *V*og, *V*ao and *V*aNfor the proposedinverter *f* = 50 Hz.

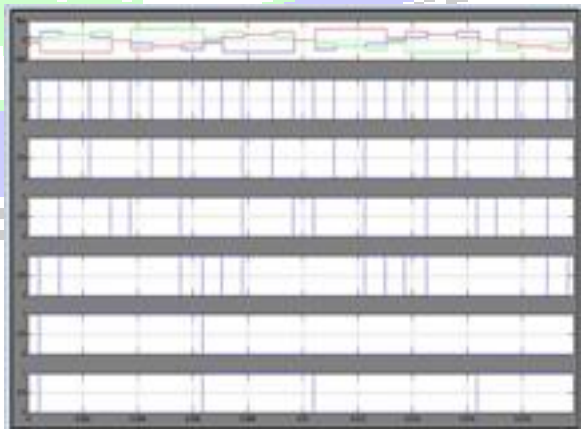


Fig. 11. Inverter's operating switching states *Sa*, *Sb*, and *Sc* with corresponding witching gate signals based on the proposed modulation method.

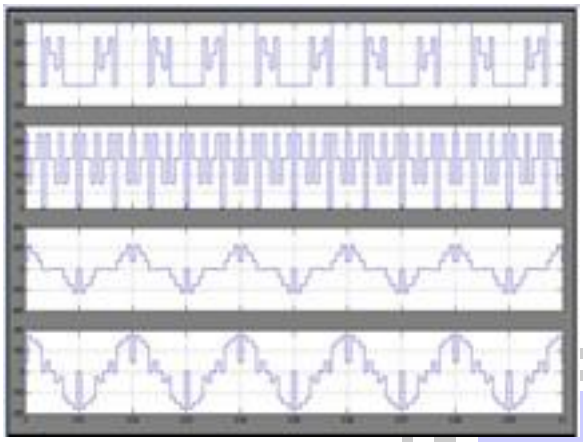


Fig.12. Simulated waveforms of *V*ab at different modulation indices for the proposed inverter: (a) *Ma* = 0.9, 1.05, and 1.15 and (b) *Ma* = 0.8 and 1.3

VII. CONCLUSION

A new topology of the three-phase nine-level multilevel by using fuzzy logic controller. The proposed topology results in reduction of installation area and cost. The fundamental frequency staircase modulation technique was comfortably employed and showed high flexibility and simplicity in control. Moreover, the proposed configuration was extended to *N*-level with different methods. Inverter was introduced. The suggested configuration was obtained from reduced number of power electronic components. The obtained simulation and hardware results met the desired output. Hence, subsequent work in the future may include an extension to higher level with other suggested methods. For purpose of minimizing THD%, a selective harmonic elimination pulse width modulation technique can be also implemented.

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