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# LOW DENSE AND LOW POWER BUS ARCHITECTURE USING MODIFIED ETI FOR SERIAL LINKS

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**ABSTRACT**:In this project, embedded transition inversion (ETI) is proposed to reduce bit transitions in Serializing parallel buses. Imply power can be reduced further. This project proposes an embedded transition inversion (ETI) coding scheme that uses the phase difference between the clock and data onto the transmitted serial data to tackle the problem of the extra indication bit as in case of Transition Inversion Coding (TIC).The technique considers a buffer of data to be a collection of bitstreams running in parallel over multiple lines. The transitions are counted in a bit serial fashion and used to determine whether the transitions in any given bitstream have to be inverted. This way the data running on any given line sequentially is encoded such a way it will have a reduced number of transitions.The technique is implemented in an optimized fashion using pipelining so that it can be used in practical systems with only a slight compromise in performance. This is achieved by calculating the decision using as the data is being loaded into the buffer and doing the encoding on the fly. This is one aspect which is lacking in most existing algorithms as they are not amenable to low delay implementation. In this paper,B2I(bit2 inversion) block is replaced with bulk of xor gates. Furthermore, area can be reduced with this enhancement when compared to existing ETI scheme. The simulations are done by Xilinx 14.5 software to get efficient output. The proposed system result analysis shows better than the existing method.
**Keywords**:ETI, TIC, Phase encoding, Tackle, B2I, Buffer, pipelining,Serializedbufferand optimization.

**INTRODUCTION**: Low power design, in a system perspective, happens at all levels of the digital electronic system stack. It is being done from the lowermost device level design to the topmost software design. And there are the intermediate levels where a lot of effort is being expended to make systems run at low power, keeping the compromise in performance to be minimum. The increasing density of the integrated circuits as postulated by Moore's law makes it even more important to have low power systems since the power supply for such a dense integrated circuit may not keep track in size with the miniaturization of the electronic components. Hence research is being made at all levels of a system stack. A system can consist of multiple components. They can be broadly classified and a communication framework designed between them.Each component in a system needs to communicate with each other throughsome form of a communication bus mechanism which will be part of the componentitself.The bus mechanism itself is standardized into multiple busses each of which service to different parts of system.

**BUS SCHEMES**: There are four types of bus schemes, including parallel (P), serial (S), encoding followed by serial (ES), and serial followed by encoding (SE) as shown in Fig1. The bitstream in this paper refers to the transmitted data in each wire of the input parallel bus. The AF analysis results of serializing two bitstreams into a single output. The proposed ETI coding uses SE scheme.The switching activity of our proposed ETI scheme is lower than the ES scheme for microprocessors and video processing.

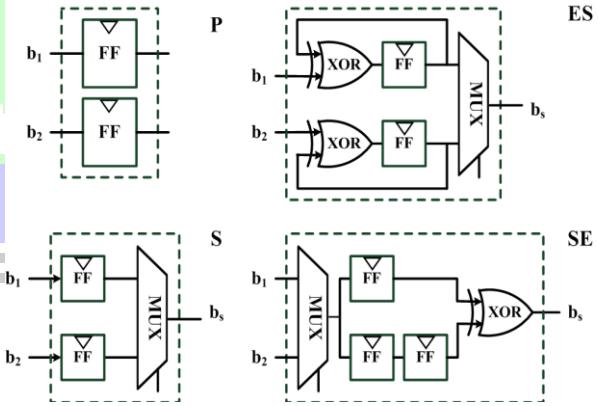


**Fig**1: Four types of bus schemes :P,S,ES and SE.

**EXSITING TECHNIQUE TO DESIGN BUS:**
(TIC) technique is used to reduce switching activity for random data. This technique counts the transitions in the data word and inverts the transition states if the

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number of transitions in a data word is more than half of the word length. This scheme sets the current bit in the serial stream to be the same as the previous encoded bit when there is notransition.Otherwise, it is set to the inversion of the previous encoded bit. A transition indication bit is added in every data word. This extra bit not only increases the number of transmitted bits but also increases the transitions and latency. A serial link on-chip bus architecture is proposed to lower interconnect power. Serialization reduces the number of wires and leads to a larger interconnect width and spacing. A large interconnect spacing reduces the coupling capacitance, while the wider interconnects reduce the resistivity. A significant improvement in the interconnect energy dissipation is achieved by applying different coding schemes and their proposed multiplexing techniques. However, the power reduction decreases when the degree of multiplexing increases. The embedded transition inversion (ETI) coding scheme solve the issue of the extra indication bit.This scheme eliminates the need of sending an extra bit by embedding the inversion information in the phase difference between the clock and the encoded data. When there is an inversion in the data word, a phase difference is generated between the clock and data. Otherwise, the data word remains same and there is no phase difference between the clock and the data. This ETI coding scheme reduces transition by 31% compared with the SE scheme.The improvement of transition reduction is 19% compared with that of the TIC.

**PROPOSED TECHNIQUE:**

In a word-length,ifdataword exceeds the threshold Nth(half of the word length), the bits in the data word should be encoded. Otherwise, the data word remains the same.When an encoding is needed in a data word, this method checks every two-bit in the data word. Every two bit in the serial stream is combined as a base to be encoded. In this case, the b11b21 is a base and the b31b41 is another base. The 2-bit in a base is denoted as b1b2 and the encoded output is denoted as be1be2. When the Ntin a data word is less than Nth, b1b2 remains unchanged. Otherwise, we perform the inversion coding and the phase coding.

**1) Inversion coding:**For the inversion coding, the bitstreams “01” and “10” are mapped to “00” and “11,” respectively. The bitstreams “00” and “11” are mapped to “01” and “10,” respectively. For the phase coding, we embed the inversion information in the phase differencebetween the clock and the encoded data.

The inversion encoding operation can be expressed as

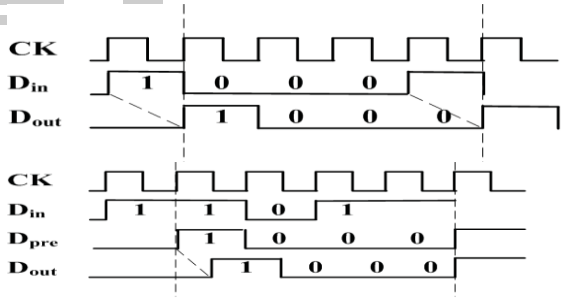
$$b_{e1} = b_1$$

$$b_{e2} = \begin{cases} b_2, & \text{with} \quad N_t < N_{\text{th}} \\ !b_2, & \text{with} \quad N_t \geq N_{\text{th}}. \end{cases}$$

Since this operation is on a two-bit basis and only the second bit is inverted, it is called bit-two inversion (B2INV).

**2) Phase Coding**: The ETI coding uses the phase difference between the data and the clock to encode the indication information. The $ETI_{pre}$ has the same data word as the TIC, except that it removes the extra bit bex. Removing the bexleaves eight sets of data words that are exactly the same. For example, there are two “1000” data words after theETIpre coding.

Within every data word duration, the phase differencebetween the data and the clock distinguishes these twodatawords, as Fig.2 illustrates. Same *D*out “1000” in Fig. 2(a) and (b) is obtained from *D*in “1000” and “1101”without and with inversion. A half clock cycle differencebetween*D*outand CK is shown in Fig.2(b), indicating that *D*inhas been encoded. The *D*out and CK are aligned in Fig. 4(a),indicating that *D*in has not changed. *D*out “0001” is the same in Fig. 2(c) and (d) from *D*in “0001” and “0100” withoutand with inversion. This approach is able to identify whether*D*out has been encoded or not as long as there is a half cycledelay between the *D*out and CK. Although the phase difference can distinguish most of the data words of ETIpre, this methodcannot be used for “0000” or “1111” because there is notransition inside the data word. Under the inversion conditionfor these two data words, the “0000” and “1111” change to“1000” and “0111”, as shown in the last column of Table I.Thecorresponding waveforms are shown in Fig.3 for thesetwo data words. The first bit of *D*out in the “1000” and “0111”is aligned with CK and the duration of the bit is only half ofthe clock cycle.



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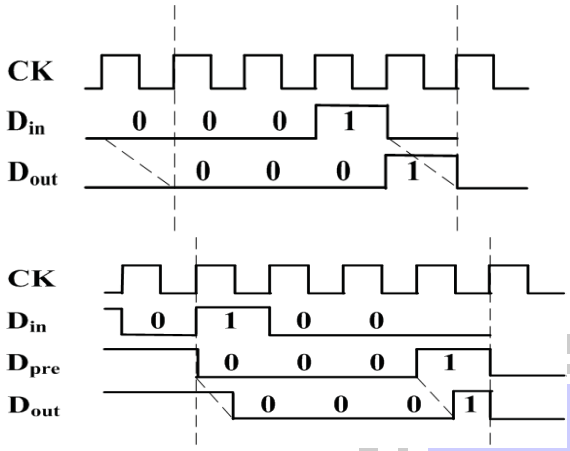


Fig.2. (a)*D*out "1000" obtained from *D*in "1000" without encoding,(b) from *D*in "1101" with encoding. (c)*D*out "0001"obtained from *D*in"0001"without encoding and(c) *D*in "0100" with encoding

The checktransition block is used to detect the numberof the transitions, is shown in Fig.5.The WL indicator block counts thelength of the data word and generates a high signal at the first bit of the data word.This signal is used to reset the adder andthe D-flip-flop (D-FF).Th

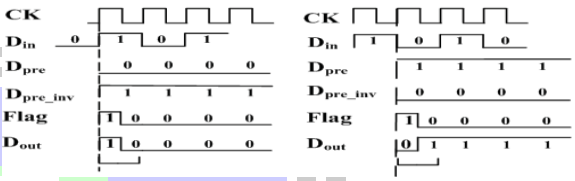


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Fig.3. Waveform example for special data words ("0000" and "1111")

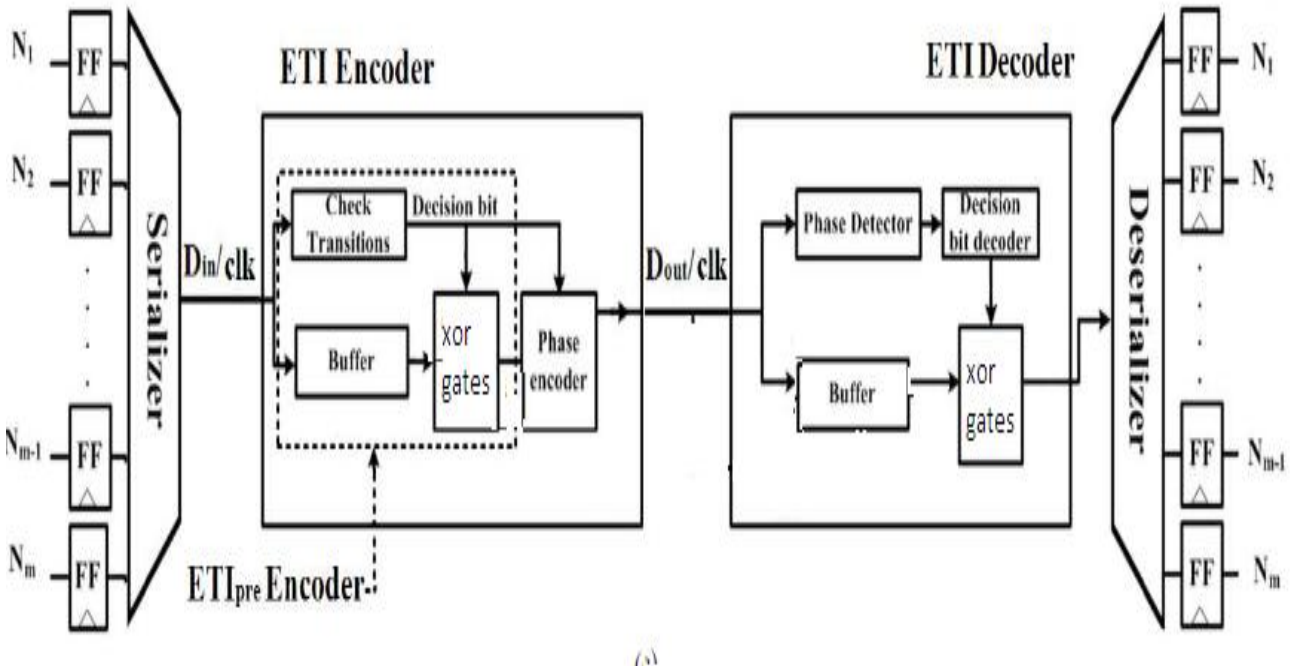


**Fig** 4: Proposed Overall architecture of the ETI scheme.

DFF stores the previous bit that isused to XOR with the current bit for transition checking. Theadder block calculates the number of transition in a data wordand sets the decision bit to high when the $Nt \geq N$th.

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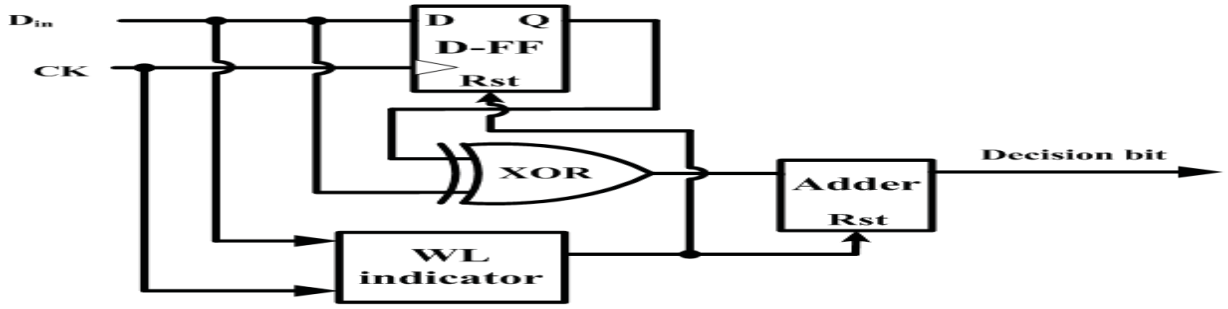


Fig.5 Check Transition Block

**ETI Decoder**:

The ETI encoder generates the phase difference between the clock and the data word. Normally, a PD identifies an earlyor delayed phase. A variety of PDs could detect the phase difference. This paper adopts the commonly used Alexander Phase Detector[PD]. The Alexander PD architecture is shown in Fig. 3 (a), which uses three consecutive clock edges to generate four sampling signals (S0, S1, S2, and S3). The PD is controlled by the clock CK and input data Din. When the clock CK andinput data Din are valid, the PD is activated to identifythephase relation between the clock and the data. The PD candetermine whether a data transition exists from the conditionthat the clock leads or lags the data. Let S1,S2,S3,S4,S5,S6,S7,S8 be the data signals.If the clock leads the data(early conditions),the signal S1 ⊕S8 is high and the S2 ⊕S8is low. Conversely, if the clock lags the data (late conditions),thesignal S1⊕S8 is low and S2⊕S8 is high. Thus, S1⊕S7 and S2⊕S6 could provide the clock and data relation are related.

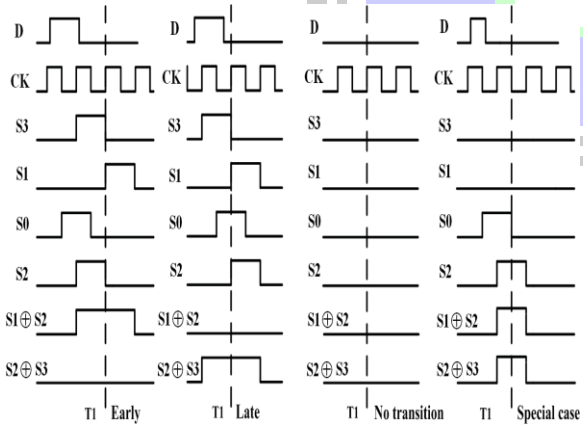


Fig 6: clock and phase difference for determining the coding state.

| S1⊕S8 | S2 ⊕S8 | Clock | Coding state |
|---|---|---|---|
| High | Low | Early | Has not been encoded |
| Low | Low | No transition | |
| Low | High | Late | Has been encoded |
| High | High | Special case | |

Table 1: Meaning of different phases

**MODIFICATION FROM PROPOSED TECHNIQUE**

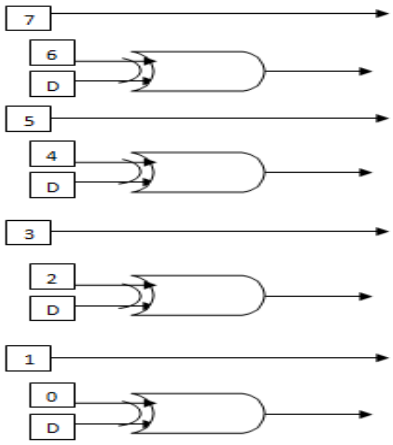


Fig 7.An array of XOR gates to invert the data

. The B2INVIinthe proposed method is removed,since it requires D-Flip Flop ,NOTgate,AND gate and multiplexer in order to invert the data, if transitions to the data are high.Instead of using this B2INV block,abulk of XOR gate combinationsisused in this project.

**RESULT:**

**EXISTING:**

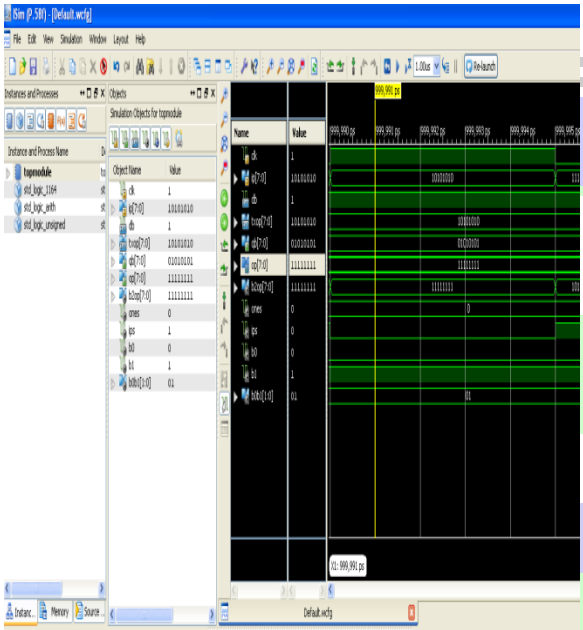

Fig 8. Simulation Result of the Existing ETI Scheme

**PROPSOED:**

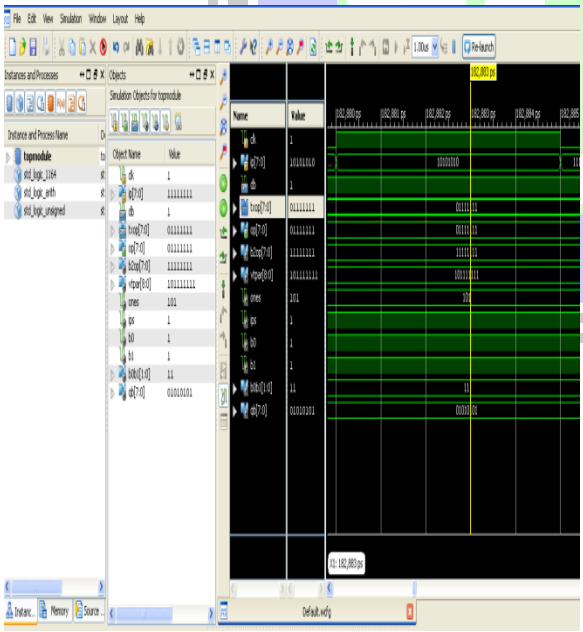

Fig 9 Simulation Result of the Proposed ETI Scheme

| PARAMETER | AREA | POWER (mW) |
|---|---|---|
| EXISTING | 403 | 414 |
| PROPOSED | 382 | 198 |

Table 2:Comparison of Existing and Proposed ETI Scheme

**CONCLUSION:**

The proposed ETI scheme achieves greater area reduction than the existing ETI scheme using XOR gate architecture. The ETI technique is proposedto reduce the extra bit used for the TIC scheme and also reduces the energy dissipation.This scheme uses the phase difference between the data and clock to indicate the bit inversion.By adopting a new architecture for B2I, an improved and area optimized XOR block is implemented.This enhanced technique is more useful in multipurpose applications due to the reason that it has low power consumption and low area overhead factors.

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