



DESIGN OF HIGH PERFORMANCE FULL ADDER CIRCUIT USING GDI TRANSISTOR LOGIC

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ABSTRACT: The current age of technology advancement it is necessary to design different new concepts to reduce area of the cell as well as power consumption. The adders are always meant to be the most fundamental requirements for process of high performance and other multi core devices. Novel circuits for XOR/XNOR and simultaneous XOR-XNOR functions are proposed in these papers. In terms of the power consumption are highly optimized in delay, due to low output consumption and low short circuit power dissipation. In this we proposed the six new hybrid I-bit full adder (FA) circuits are based on the novel full swing XOR-XNOR or XOR/XNOR gates.

KEY WORDS: Transistor sizing method, particle swarm optimization (PSO), Full adder (FA), XOR/XNOR.

I.INTRODUCTION

VLSI systems are having many operations like fundamental arithmetic operation in addition is one of the common and widely used operations. Such as arithmetic operations are subtraction, multiplication, division, address calculation etc. Utilizing binary adders the full adder is structured and enhancing 1-bit full adders execution assumes a vital job in VLSI. Distinctive assortments of full adders abuse totally unique rationale structures and advances. The battery which is having demand of current history the devices are driven and portable, low power and area efficient devices they must need an implementation. As indicated the multiplying module focus upon silicon wafer in every 3 years by Moore's law. In this system of interconnection limited circuit are having thickness on a chip, therefore transistor door length is decreased to huge dimension. The structured applications of today are

in the range 2nm. Chip is essential and basic piece of numerous items are required for ordinary.

For example, home apparatuses, radio and PCs frameworks. Span of transistor was confined in wonders short channel impacts are incorporate of bearer impact of hot, gate prompted hindrance bringing down, impact and burrowing of oxide thickness. In corruption of gadget execution and gadget lifetime at littler door length is because of expanded electric field. The central piece of chip of a transistor. Chief test was minuscule issues at nanometer go is ultra rapid; control dissemination and supply voltage. Lower control prompts lesser power supplies, less exceptional batteries [2].

Low power and High speed are the plan exchange offs in VLSI industry. As far back as its beginning, the plan of full adders which shapes the essential building squares of all computerized VLSI circuits has been experiencing a significant enhancement,

being roused by three fundamental structure objectives, viz. limiting the transistor tally, limiting the power utilization and expanding the speed. Most of the VLSI applications, for example, advanced flag preparing and microchips, utilize number-crunching activity. Expansion, subtraction, augmentation, and increase and collect (MAC), are instances of the most normally utilized activities. The development of compact gadgets like PDAs, PDAs, and so on, request fast handling capacities that additionally expend less power. The 1-bit full adder is the building square of these activity modules. In this way, improving its execution is basic for upgrading the general module execution. In this paper, we present a novel 1-bit full-adder cell utilizing XOR-XNOR circuit, which offers quicker activity, and devours less power than the other proposed full-adder cell dependent on XOR-XNOR gate [1].

The structure paradigm in a full adder cell was normally different overlap. The transistor tally was, obviously, an essential concern which to a great extent influences the plan intricacy of many capacity units, for example, Algorithmic rationale unit (ALU) and multiplier. The restricted power supply capacity of present battery innovation has made power utilization a vital figure in convenient gadgets. The restricted by the size of the transistors, parasitic capacitance and postponement the speed of the plan in the basic way [3]. Capacity of driving was a full adder is imperative, since, full adders are generally utilized in course setup, where the yield of one gives the contribution to other. On the off chance that the full adders need driving ability, at that point it requires extra support, which therefore builds the power scattering significant enhancement in power utilization, speed and size, however at the expense of feeble driving capacity and decreased voltage swing. In any case, decreased voltage swing has the benefit of lower control utilization.

At first the hardware began their advancement with the innovation of vacuum tubes. Be that as it may, with the assistance of Vacuum tubes just the development of electrons was contemplated. After vacuum tubes transistors and diodes were presented. Be that as it may, for bigger circuits it was hard to manufacture them in a board as they involved bigger space and devoured more power. The full adder circuit execution is subject to the methodology for structuring the circuit. The speed of activity of a circuit is in a roundabout way found with the assistance of defer time figuring which specifically relies upon the transistor check, the rationale profundity and other criteria. The power utilization relies upon the exchanging movement and the number and the transistor estimate.

The transistor measure and steering multifaceted nature knows the territory of a kick the bucket. Circuit acknowledgment for low zone has turned into a vital issue with the development of incorporated circuit towards high combination thickness and high working frequencies. Because of the critical pretended by XOR-XNOR gate in different circuits particularly in number-crunching circuits, streamlined structure XOR-XNOR circuit to accomplish little size and deferral is required. The essential worry to structure XOR-XNOR door is to get low power utilization and postponement in the basic way and full yield voltage swing with low number of transistors to execute it. An overview of writing uncovers a wide range of various sorts of XOR-XNOR doors that have been acknowledged throughout the years. The early structures of XOR-XNOR gates depended on either 4 transistors or 3 transistors that are expectedly utilized in many plans [4]. Full adder goes about as the essential square of all adders which are utilized to perform multi bit increases. There are additionally different approaches to plan the Full Adder circuit as far as

CMOS rationale [5]. With expanding request in speed and power, our principle point is to configuration Full adder circuit so it devours less power and quicker. The vast majority of the power in any circuit is being devoured by the power given to the information way of the circuit which comprises of the transistors. Subsequently by lessening the quantity of transistors we can decrease the power utilization additionally by diminishing the information way, the circuit can be made quicker.

II. RELATED WORK

The testing criteria of the rising low power and fast correspondence computerized flag preparing chips can be tended to by investigating the very much designed profound submicron transistor advancements. The execution of the fundamental number circuits to actualize complex calculations, for example, convolution, relationship and advanced sifting, characterizes the execution of numerous greater modules of Digital Signal Processors (DSPs). The semiconductor business has seen a touchy development of mix of modern interactive media based applications into portable hardware gadgetry since the most recent decade. Be that as it may, control utilization is the basic region of worry in this field and must be diminished for a specific working recurrence. Also, there is a drive by creators to take a stab at littler silicon territory, higher speed, longer battery life, and upgraded dependability in light of dangerous development of interest and prominence of convenient electronic items.

The motivation behind coordinated hardware is to pack complex electronic circuits in least territory with decrease in power dispersal and postponement. With the period of innovative progression, diminishing the quantity of transistors and ultra-low power configuration has turned into the main thrust for mix of an ever increasing number of uses without acquiring any overhead as far as silicon region. The

execution of configuration is significantly represented by three essential variables viz. zone multifaceted nature, postpone execution and consistency of interconnection. The consistency of interconnection implies the manner in which transistors are set down, directing of interconnects in the most ideal way and conforming to the tenets of format. Territory of the circuit likewise relies upon the interconnection of wires which exhaust the greater part of the region of a VLSI circuit. Diverse rationale styles have been proposed throughout the years with an exchange off of one execution angle to the detriment of other. The circuit delay is influenced by the quantity of transistors in arrangement, wiring interconnections identified with wiring capacitances, transistor sizes and number of reversal levels. Full adder usage can be accomplished by utilizing it is possible that

one rationale style or more than one rationale style. The XOR-XNOR circuits are fundamental building hinders in different circuits' particularly number juggling circuits (adders and multipliers), blowers, comparators, equality checkers, code converters, mistake recognizing or blunder remedying codes and stage identifier. The adders and multipliers being the quick number continuously calculation cells and generally utilized for some circuits of VLSI configuration are the regular research zones. A further expansion to unwavering quality and bundling issue issues have been brought with the ascent up in chip thickness and increment in power utilization of VLSI frameworks. Bundling and cooling cost of VLSI frameworks likewise runs up with high power dispersal. These days, low power utilization alongside least postponement and zone necessities is one of vital plan thought for IC originators.

Circuit acknowledgment for low power and low territory has turned into a vital issue for the development of incorporated circuit towards

exceptionally high joining thickness and high working frequencies. Because of the imperative pretended by XOR and XNOR doors in different circuits particularly in number continuously circuits, improved plan of XOR and XNOR circuit to accomplish low power, little size and low deferral is required. The essential worry to plan XOR-XNOR gate is to get low power utilization and postponement in the basic way and right yield having the least number of transistors to execute the voltage swing. XOR gate is a basic building square of advanced circuits and there is constant research proceeding to upgrade its execution. Along these lines, as far back as its origin, the structure of XOR gates frames the fundamental building square of all advanced VLSI circuits which has been experiencing a significant enhancement, being spurred by three essential plan objectives, viz. limiting the transistor tally, diminishing the power utilization and expanding the speed. Hosseinzadeh underscored that the circuit execution can be enhanced through transistor tally minimization. XOR gates assume an imperative job in advanced frameworks including math circuits, encryption circuits, comparator, equality checker, etc. Upgrading the execution of the XOR gates can altogether enhance the execution of these circuits. Many plan structures and procedures have been created to plan XOR doors with decrease in power utilization. The writing study uncovers a wide range of XOR gates that have been acknowledged throughout the years. The predominant worry to structure XOR door is to procure right yield voltage swing with least number of transistors and furthermore, execution with low power utilization and postponement in the basic way

III. EXISTED SYSTEM

The below figure (1) demonstrates the engineering of existed framework. The non full-swing XOR/XNOR circuit which is appeared in fig (1) has the power and delay as far as productive. This

structure has a yield voltage drop issue for just a single information legitimate esteem of its besides. To tackle this issue and give an ideal structure to the entry way of the XOR/XNOR, in the circuit appeared in Fig.

I was proposed. In the full swing the structure of the yield of this, the all conceivable info mixes. The basic way of the circuit on NOT gates does not have of the existed system of XNOR/XOR.

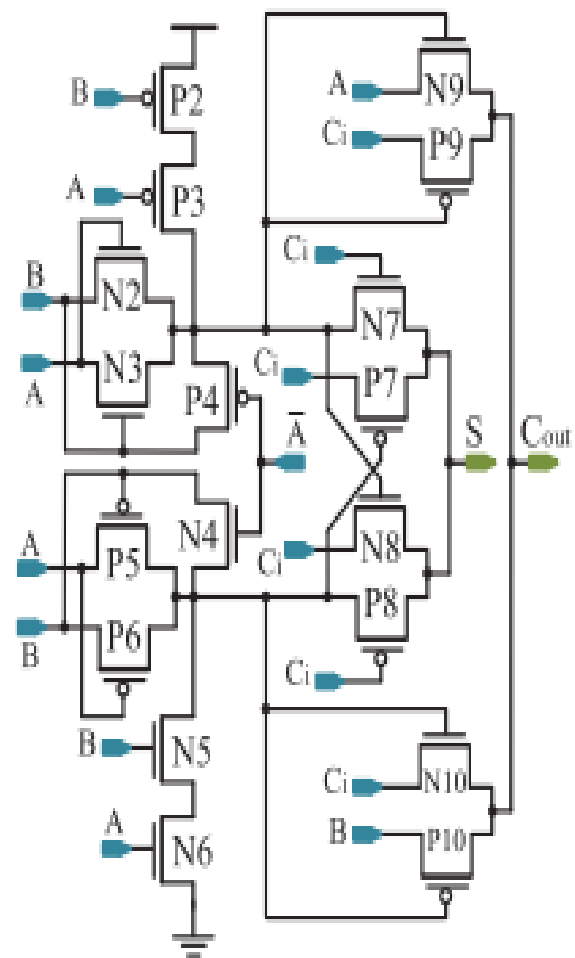


Fig. 1: EXISTED SYSTEM

The data sources are as per the following An and B which are denoted as the capacitances of the XOR circuit. These are not symmetric on the grounds side and one of these two should be related with the commitment of NOT gate. In the same way another

should be related with the scattering of nMOS transistor. In addition, the data capacitances of transistors N2 and N3 are not equal in the perfect situation (least PDP). Generally, the information relationship with transistors N2 and N3 won't impact the limit of the circuit. Hence, it is more brilliant to relate the data A, which is moreover connected with the NOT passages and to the transistor with smaller information capacitance. By doing this, the information capacitances are progressively symmetrical, and thusly, the delay and power usage of the circuit will be lessened. To light up which transistor (N2 or N3) has greater data capacitance, let us consider the condition that the wellsprings of information change from $AB = 00$ to $AB = 10$.

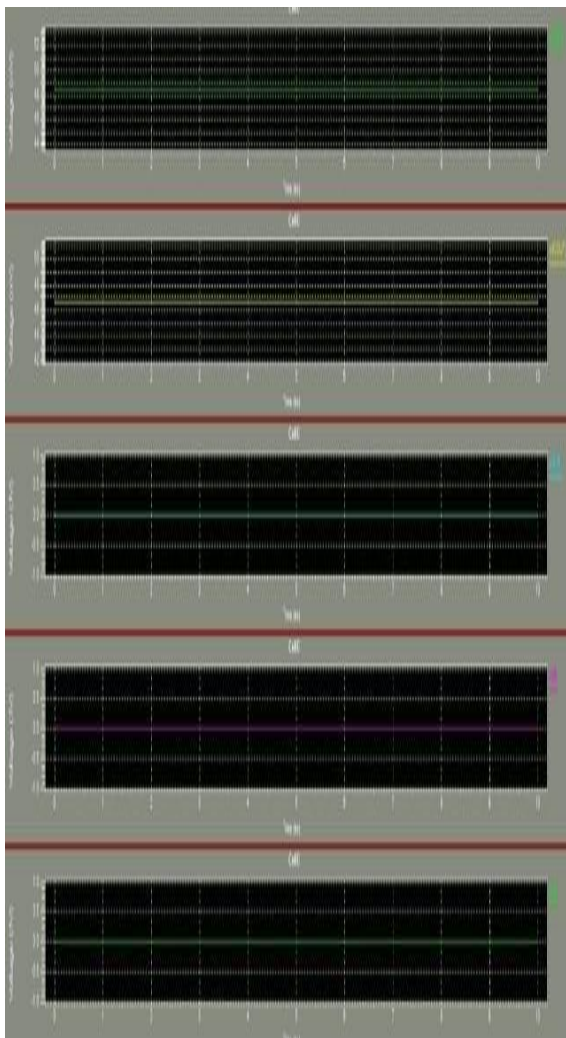


Fig. 2: EXISTED OUTPUT WAVEFORM

IV. PROPOSED SYSTEM

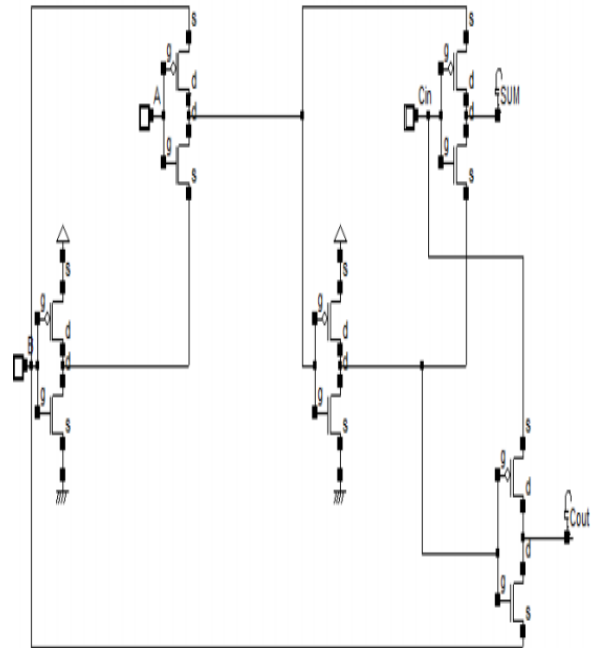


Fig. 3: PROPOSED DESIGN

The above figure (3) shows the design of proposed system. The full adder comprises of two modules, including one XOR-XNOR door, and two multiplexers. The creators give XOR-XNOR gates to enhance the execution of full adders. , these XOR and XNOR doors give awful yield rationale levels for certain information blends.

This issue can be tackled by controlling the (W/L) proportions of PMOS and NMOS transistors, which reestablishes the rationale levels to a worthy dimension. Basically, the XOR/XNOR gate produces the intensity in the full adder cell. Hence the power utilization is decreed by the full adder cell with the planning. The XOR/XNOR gates will be used in different computerized applications. In this system we use eight transistors for better purpose. Here NOT gate is used in the circuit of grounds of NOT cells. These cells should drive the delay in basic formation level. Depend on the logic style of transistor the circuits operate its function. In this circuit the power utilization is superior. The XOR-

XNOR signals are mainly associated with the full adder circuits. The XOR-XNOR contributes its signals by using multiplexers. Consequently, two concurrent signs with a similar postponement are important to keep away from glitches in the yield hubs of the FA. In this structure, the yields have been driven just by nMOS transistor, and along these lines, two pMOS transistors are associated with yields (XOR and XNOR) as cross coupled to recoup the yield level voltages.

The main issue in the XOR-XNOR circuits is having cross coupled structure. This structure will expand the intensity of the system. Not only intensity, the measure of transistor is also expanded to a level. By using two NOT gates in the system is a big issues in the system. Hence the outputs of XOR and XNOR gates will practically diminish the output stage. But the proposed system gives effective results compared to existed system.

V. RESULTS

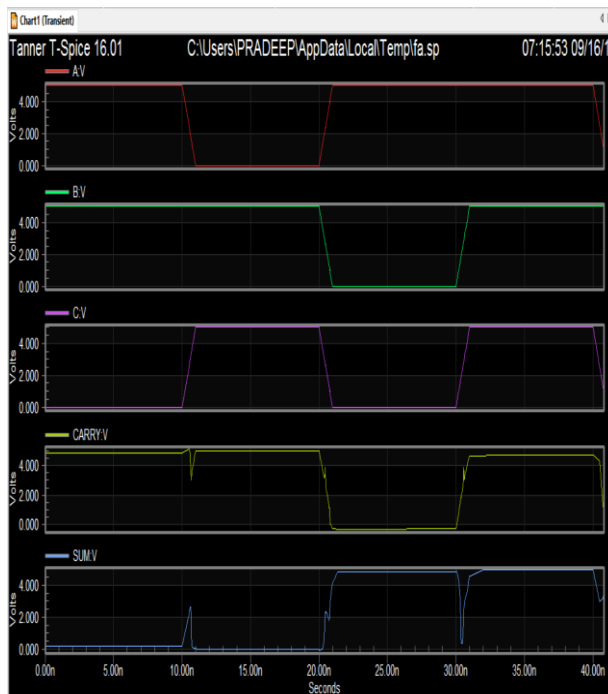


Fig. 4: OUTPUT WAVEFORM

In the proposed system, the number of transistors used is 20 and in existed system, the number of transistors used is 10.

VI. CONCLUSION

In this project, the evaluation of arithmetic circuit using GDI transistor logic full adder is proposed. This system gives effective output compared to others. Proposed XOR-XNOR gate will offer full adder cell and it is applicable in various applications. Transistor sizing in digital circuits is also done in the proposed method. High speed and energy efficient design is obtained by using proposed full adder design using XOR/XNOR circuits. All proposed FAs have normal sensitivity to variations. In future the researchers will use circuit level power management techniques. The field of circuitry will be determined depend on the low power applications.

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